Microsystems Annual Research Report

2023

CICS Edition

MTL MICROSYSTEMS TECHNOLOGY LABORATORIES

MIT.nano

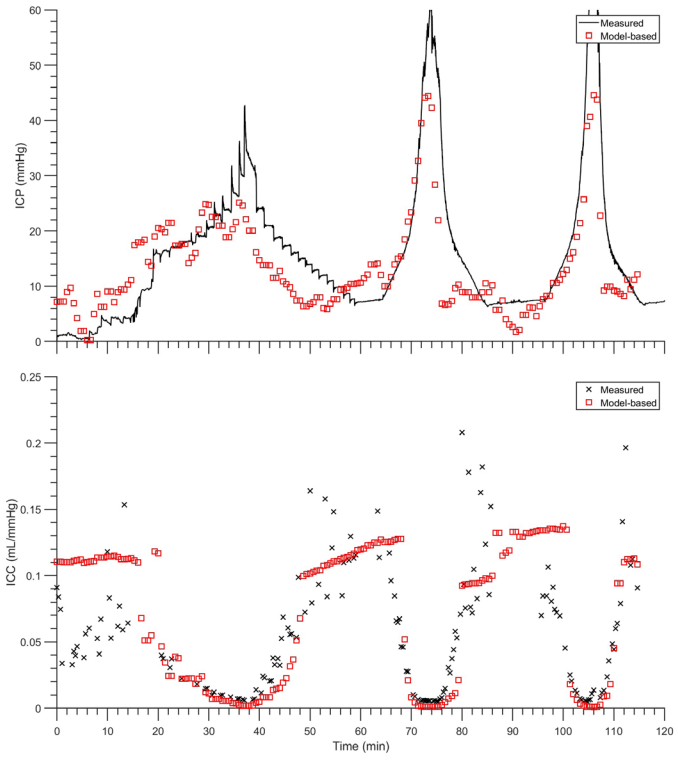
MASSACHUSETTS INSTITUTE OF TECHNOLOGY

Model-based Noninvasive Intracranial Compliance and Vascular Resistance Estimation

S. M. Imaduddin, C. G. Sodini, T. Heldt
Sponsorship: Analog Devices, Inc. via MIT Medical Electronic Device Realization Center

Existing neuromonitoring methods used for patients with severe head injury tend to be highly invasive and carry a risk of tissue damage and infection. In particular, fluid infusion/withdrawal studies via indwelling catheters are needed to determine intracranial compliance (ICC)–an index of the propensity of rise in intracranial pressure (ICP) in response to changes in cranio-spinal volume. Despite their potential to serve as early indicators of intracranial hypertension, ICC measurements are rarely performed owing to time-consuming, invasive measurement protocols. In addition, measurements of cerebrovascular resistance (CVR) to blood flow are useful in assessing cerebral autoregulation and tracking pathological vascular narrowing such as in moyamoya disease. Like ICC, however, CVR is not regularly obtained at the bedside as the requisite measurements–arterial blood pressure (ABP), cerebral arterial blood flow (CBF), and ICP–are rarely monitored simultaneously.

We have developed a noninvasive, model-based approach for ICP, ICC, and CVR estimation that is driven by subjects' ABP and CBF measurements. Our system was initially validated qualitatively in healthy adult volunteers undergoing head-up tilts. We are now in the process of quantitatively validating our approach in an animal model. ICP is raised experimentally and measurements of the ABP, CBF, ICP, ICC, and CVR are acquired. Model-based estimates of the ICP, ICC, and CVR are then compared to invasive reference measurements. Initial results suggest that our model-based estimates are close to the reference measurements; further validation is now underway. Simultaneously, we have deployed our data collection approach at Boston Children's Hospital to evaluate the system's efficacy in pediatric patient cohorts. If proven successful, our approach can pave the way towards convenient and safe neuromonitoring across a wide spectrum of pathologies, patient age, and disease severity.

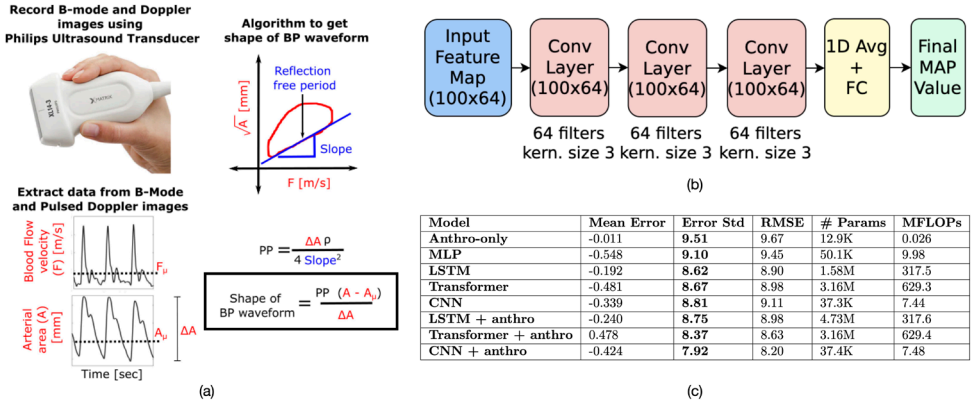


▲Figure 1: Illustration of invasive measurements and model-based estimates of ICP and ICC, respectively, for one subject in the rabbit model.

Cvb Machine Learning for Arterial Blood Pressure Prediction

H. Wang*, J. Zheng*, A. Chandrasekhar, J. Seo, A. Aguirre, S. Han, C. G. Sodini, H.-S. Lee
Sponsorship: MIT J-Clinic, Philips, Analog Devices, MIT-IBM Watson AI Lab, NSF CAREER Award

High blood pressure is a major risk factor for cardiovascular disease. As such, accurate blood pressure (BP) measurement is critical. Clinicians measure BP with an invasive arterial catheter or via a non-invasive arm or finger cuff. However, an arterial catheter can be painful for the patient and not ideal outside an intensive care unit (ICU). Cuff-based devices are non-invasive, but they cannot provide continuous measurement, and they measure from peripheral blood vessels whose BP waveforms differ significantly from those closer to the heart. Hence, there is an urgent need to develop a measurement protocol for converting easily measured non-invasive data into accurate BP values. In this work, we propose a non-invasive approach to predict BP from arterial area and blood flow velocity signals measured from a Philips ultrasound transducer (XL-143) on large arteries close to heart. We developed the protocol and collected data from 72 subjects. The shape of BP (relative BP) can be theoretically calculated from these waveforms, but there is no established theory to obtain absolute BP values. Therefore, we further employ data-driven machine learning models to predict the mean arterial blood pressure (MAP), from which the absolute BP can be deduced. We propose several different machine learning algorithms to optimize the prediction accuracy. We find that long short-term memory (LSTM), transformer, and one-dimensional convolutional neural network (1D-CNN) algorithms using the BP shape and blood flow velocity waveforms as inputs can achieve 8.6, 8.7, and 8.8-mm Hg average standard deviation of the prediction error, respectively, without anthropometric data (age, sex, heart rate, height, weight). Furthermore, the 1D-CNN model can achieve 7.9-mm Hg when anthropometric data are added as inputs, improving upon an anthropometric-only model of 9.5-mm Hg. This machine-learning algorithm can be a software modality that converts ultrasound data to MAP values to help physicians make clinical decisions.



Model	Mean Error	Error Std	RMSE	# Params	MFLOPs
Anthro-only	-0.011	**9.51**	9.67	12.9K	0.026
MLP	-0.548	**9.10**	9.45	50.1K	9.98
LSTM	-0.192	**8.62**	8.90	1.58M	317.5
Transformer	-0.481	**8.67**	8.98	3.16M	629.3
CNN	-0.339	**8.81**	9.11	37.3K	7.44
LSTM + anthro	-0.240	**8.75**	8.98	4.73M	317.6
Transformer + anthro	0.478	**8.37**	8.63	3.16M	629.4
CNN + anthro	-0.424	**7.92**	8.20	37.4K	7.48

(c)

▲ Figure 1: (a) The whole pipeline of using machine learning-based algorithms to get BP waveforms from ultrasound data (b) CNN model architecture (c) Performance summary.

FURTHER READING

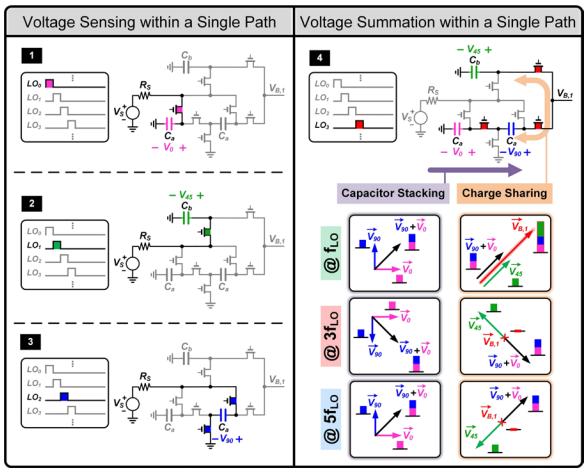
- V. Novak and L. Mendez, "Cerebral Vasoregulation in Diabetes," (version 1.0.0), *PhysioNet, 2020. https://doi.org/10.13026/m40k-4758.*
- J. Zheng, H. Wang, A. Chandrasekhar, A. Aguirre, S. Han, C. G. Sodini, and H.-S. Lee, "Machine Learning for Arterial Blood Pressure Prediction," *CHIL*, 2023.

Harmonic-resilient Fully Passive Mixer-first Receiver for 5G NR Applications

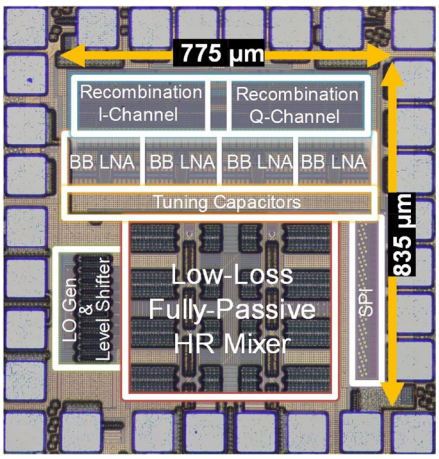
S. Araei, S. Mohin, N. Reiskarimian

Software-defined radios (SDRs) are versatile radio receivers that offer the promise of an all-in-one communication radio for multiple standards such as Bluetooth, Wi-Fi, and 5G new radio. To tackle the issue of interference, SDRs require a band-select filter with a widely tunable center frequency and bandwidth. However, integrating such a filter on-chip is challenging. In recent years, the mixer-first architecture has emerged as a promising candidate for SDRs as the passive mixer's reciprocity nature provides such a filter at the antenna interface by upconverting the baseband impedance to the radio-frequency (RF) domain. This inductor-less sharp-filtering scheme enhances the receiver's tolerance to near out-of-band blockers in a small form factor. Additionally, the mixer-first approach allows for precise and independent control over the center frequency and bandwidth of the filter. However, harmonic mixing can cause signals located at or around the harmonics of the local oscillator (LO) to downconvert to the baseband and readily saturate the subsequent baseband amplifiers. Thus, it is essential to suppress the LO signal's harmonic content.

In this work, we propose a low-loss all-passive harmonic-resilient and blocker-tolerant mixer-first receiver. This design exploits a co-design of charge-sharing and capacitor stacking to form a harmonic rejection filter right inside the mixer, thus eliminating the harmonic blockers before hitting the active stages. The proposed harmonic filtering technique requires no additional circuitry beyond extra switches and benefits from technology scaling. The fabricated 45-nm silicon-on-insulator (SOI) prototype RX, with a silicon area of 0.65 mm2, operates across a wide frequency range, from 250MHz to 2.5GHz, and tolerates >10dBm 3rd harmonic blocker power, which is 40× larger than a state-of-the-art broadband harmonic rejection receiver. The proposed architecture offers high linearity against close-in and far-out blockers while also maintaining the widely tunable nature of mixer-first receivers, bringing us one step closer to realizing the vision of all-in-one communication radios.



▲ Figure 1: Time-domain operation of the proposed low-loss fully passive harmonic rejection mixer.



▲ Figure 2: Die micrograph of the proposed harmonic rejection receiver.

FURTHER READING

- S. Araei, S. Mohin, and N. Reiskarimian, "An Interferer-Tolerant Harmonic-Resilient Receiver with >+10dBm 3rd-Harmonic Blocker P1dB for 5G NR Applications," *IEEE International Solid- State Circuits Conference (ISSCC)*, San Francisco, CA, pp. 18-20, 2023.
- S. Araei, S. Mohin, and N. Reiskarimian, "Realization of Low-Loss Fully-Passive Harmonic Rejection N-Path Filters," to be presented at *IEEE International Microwave Symposium (IMS)*, San Diego, CA, Jun. 2023.

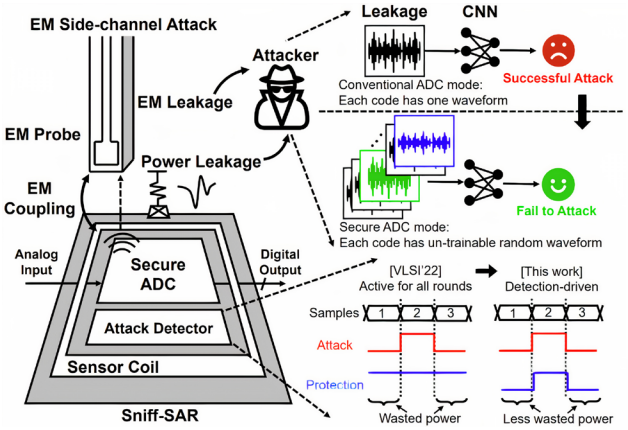
Sniff-SAR: A 9.8fJ/c.-s 12b Secure ADC with Detection-driven Protection Against Power and EM Side-channel Attack

R.-C. Chen, A. P. Chandrakasan, H.-S. Lee
Sponsorship: Center for Integrated Circuits and Systems, DARPA

As shown in Figure 1, sensitive and confidential information can be stolen from an analog-to-digital converter (ADC) by electro-magnetic side-channel attacks (EMSA) or power side-channel attacks (PSA). An EM probe can measure the EM side-channel information of the ADC. An attacker can obtain the power side-channel information by measuring the power traces of the ADC. There are two challenges for secure ADCs. First, to address the security concerns, secure ADCs have non-negligible overheads in energy and area, which is not ideal for resource constrained applications such as the Internet of Things. The protection scheme is typically always-on even if the side-channel attacks are not performed. Second, neural network-based side-channel attacks are becoming more powerful, making existing protection less robust. To address these two challenges, this work proposes the first detection-driven ADC secure against both power and EM side-channel attacks. The ADC normally operates in an energy-efficient switching mode. When an EMSA or PSA is detected, secure switching is enabled that renders the ADC very protected from neural network-based attacks.

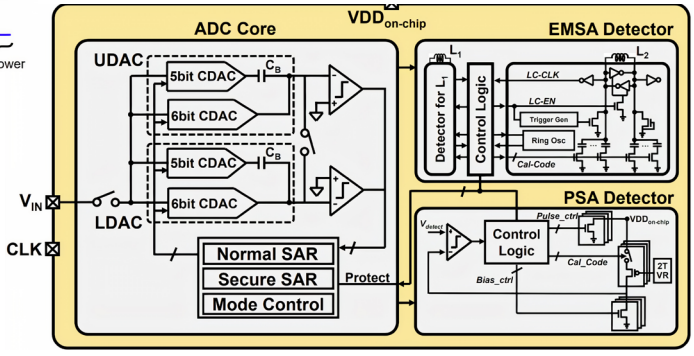
Figure 2 shows the system architecture of the Sniff-SAR with detection-driven protection. The EMSA and PSA detectors capture the attempt of side-channel attacks. The ADC core normally operates in the unprotected SAR mode, which is faster and more energy-efficient. EMSA and PSA detectors check for the side-channel attacks periodically; once they notice that the ADC is under attack, the ADC activates the secure SAR mode against both EMSA and PSA.

Fabricated in the 65-nm LP process, the Sniff-SAR occupies 0.075 mm² (Figure 2). Compared with always-on protection, we introduced detection-driven protection. Moreover, a new switching scheme is implemented, which is practically untrainable using neural networks. This work also demonstrates the highest sampling rate and best figure of merit (FoM) in secure ADCs by a duty cycling for both detectors. The secure SAR achieves an FoM of 9.8fJ/c.-s., which is comparable to the state-of-the-art energy-efficient unprotected ADC using similar technology.



◀Figure 1: Side-channel security challenges of ADCs and detection-driven protection based on randomization

▼Figure 2: System architecture of the side-channel-secure ADC with detection-driven protection



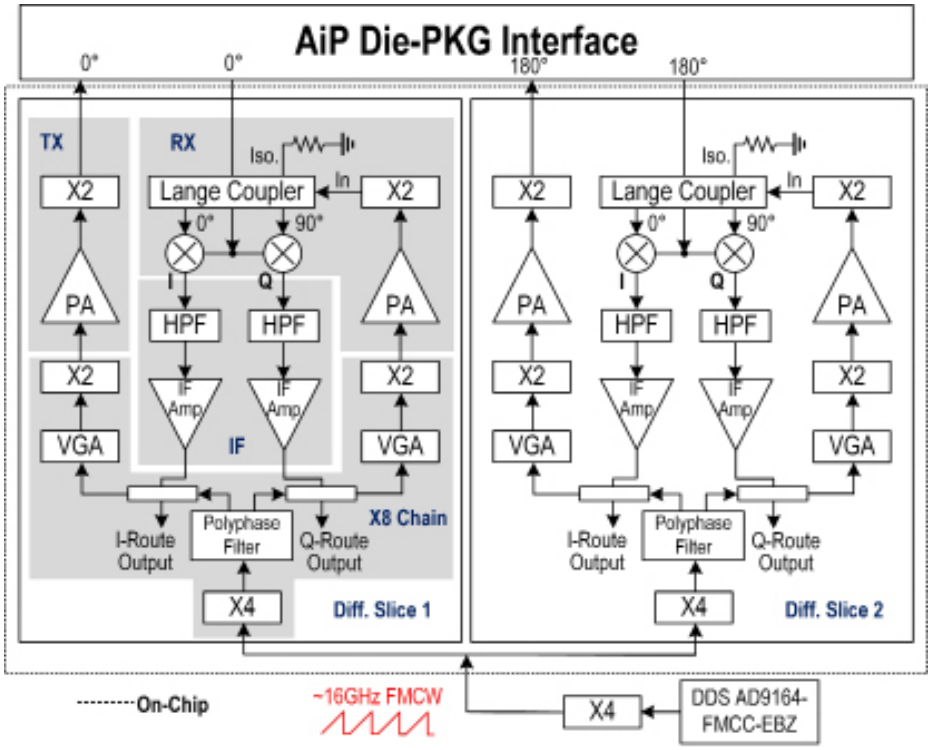
FURTHER READING

- R. Chen, A. Chandrakasan, & H.S. Lee, "Sniff-SAR: A 9.8 fJ/c.-s 12b Secure ADC with Detection-driven Protection Against Power and EM Side-channel Attack", *2023 IEEE Custom Integrated Circuits Conference* (CICC) (pp. 1-2). IEEE, April 2023.
- R. Chen, H. Wang., A. Chandrakasan, & H.S. Lee, "RaM-SAR: A Low Energy and Area Overhead, 11.3 fJ/conv.-step 12b 25MS/s Secure Random-Mapping SAR ADC with Power and EM Side-channel Attack Resilience," *2022 IEEE Symposium on VLSI Technology and Circuits* (VLSI Technology and Circuits) (pp. 94-95). IEEE, June 2023.

A 260GHz Transceiver with High-efficiency Antenna-in-package on 22nm FinFET Process

X. Chen, G. Dogiamis, R. Han
Sponsorship: Intel Corporation

CMOS-based on-chip antenna for sub-THz radiation suffers from its inherently low radiation efficiency, due to extremely small thickness of dielectric stack, and lossy silicon substrate. Transistor cut-off frequency (fmax) in nowadays mainstream CMOS processes further introduces significant hurdles for generating high radiated power at sub-THz regime, especially when the operating frequency exceeds 200GHz. This work shows a 260GHz transceiver design with high-efficiency antenna-in-package (AiP) design, based on Intel 22nm FinFET process. Simulation shows the highest radiation efficiency among all other reported CMOS works under the same frequency. An on-chip 260GHz transceiver is designed to pair with the AiP. The whole system shows a simulated wide bandwidth and decent radiated power, which translates to high ranging resolution with long detection range for FMCW radar detection.



▲ Figure 1: 260GHz Transceiver System Diagram.

Retro-backscatter THz ID: With Energy Harvester and BPSK Backscatter

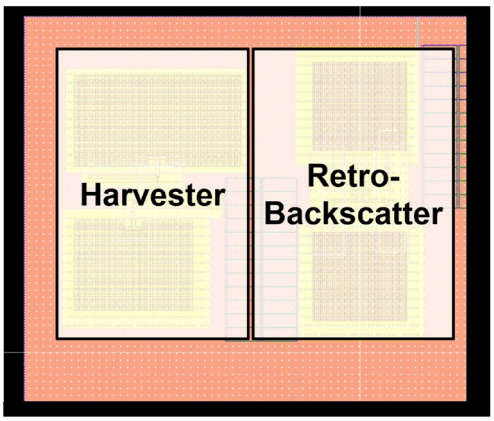
M. Jia, D. Sheen, R. Han, A. P. Chandrakasan
Sponsorship: Intel University Shuttle, NSF

Radio-frequency identification (RFID) tags have become a ubiquitous technology for tracking, authentication, localization, supply-chain management, and more. Nevertheless, commercial RFID chips currently rely on the external antenna or inductor packaging to enable efficient coupling of RF waves. Unfortunately, this design significantly increases the tag's overall size, rendering it unsuitable for attachment to small objects like medical pills, tooth implants, and semiconductor chips. An additional cost is associated with the chip packaging, which takes up to two-thirds of the total tag cost. Therefore, there is a pressing need for fully passive, particle-sized cryptographic chips that require no external packaging to allow secure and ubiquitous asset tagging. Besides, we want users to be able to read our tags at a long distance and from a flexible angle. At the same time, a single source input will significantly reduce the cost of the tag reader itself.

To address these challenges, we propose an entirely new version of the terahertz (THz) ID called Retro-backscatter THz ID. Firstly, we proposed a fully passive retro-backscatter system with binary phase-shift keying (BPSK) modulation to enhance the operating distance of the tag. Currently, RFID systems suffer from a major drawback whereby reflected power is radiated omnidirectionally, dissipating valuable re-radiated power away from the desired receiving reader, which drastically limits the tag's operating range. Additionally, our proposed retro-backscatter design effectively mitigates the problem of phase sensitivity of the backscatter array and offers users the ability to read the tag from a more flexible angle.

Furthermore, we introduce a THz harvester and direct current-direct current converter that enables a single THz signal input, thus allowing for both energy harvesting and tag functionality, to also reduce the cost of the reader. We also integrate an ultra-low-power digital dedicated processor into the THz-ID chip, which provides high-security compact asymmetric encryption.

▲ Figure 1: Multi-functional electromagnetic design.



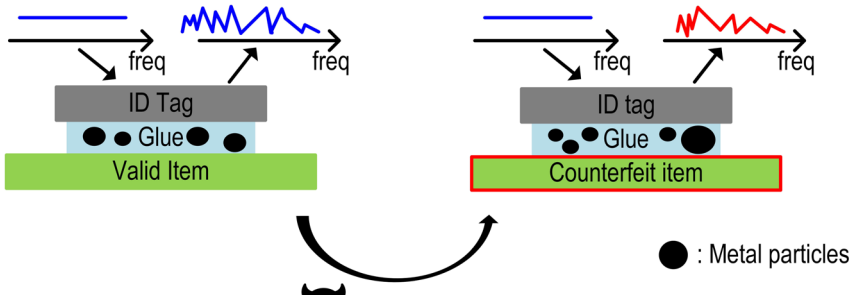
▲ Figure 2: Partial layout of the proposed Retro-backscatter THz ID.

A Physically Unclonable Anti-tampering THz-ID Tag

E. Lee, M. Jia, A. P. Chandrakasan, R. Han
Sponsorship: Korea Foundation for Advanced Studies, NSF (SpecEES ECCS-1824360)

Wireless radio-frequency identification (RFID) tags are becoming more popular, particularly in supply chain management and item authentication. For these tags to be widely used, they must be small, cost-effective, and easily adaptable to any object without requiring complicated packaging. Recently, the first demonstration of a 1.6 mm2 terahertz (THz) wireless tag that can authenticate items without packaging was presented. This tag is enabled through the on-chip antennas and low-power bi-directional communication via zero-power THz detecting and THz backscattering. Despite its ability to authenticate items, the wireless tag is still susceptible to tampering since an attacker could remove the ID tag from the authentic item and attach it to a counterfeit one. This could make it difficult for the reader to distinguish between genuine and fake items.

The study aims to address the security vulnerability of wireless tags by developing a small, packaging-free tag that has anti-tampering features. Our approach involves utilizing the material properties of the adhesive interface between the THz-ID tag and item to generate and extract a distinctive THz electromagnetic signature. Once affixed to an item, the anti-tampering ID tag generates a distinct electromagnetic signature. This signature is obtained by interrogating the tag using a reader, and THz response is stored within the data set. If a hacker attempts to remove and reattach the tag to a different surface, the electromagnetic signature will be disrupted. The reader can detect this tampering (Figure 1). Replicating the unique THz signature generated by the interaction between the ID tag, surface, and adhesive materials is a difficult and expensive task for hackers due to the random distribution of the signature. This makes it impractical for them to clone the tag. While this project is still in-progress, this system will advance the utilization of the THz spectrum for secure authentication of self-powered Internet of Things and wireless tags.



▲ Figure 1: The scenario of tampering attacks on THz anti-tampering ID tags.

FURTHER READING

- M. I. Ibrahim et al., "29.8 THzID: A 1.6mm2 Package-Less Cryptographic Identification Tag with Backscattering and Beam-Steering at 260GHz," *IEEE International Solid-State Circuits Conference*, San Francisco, CA, pp. 454-456, 2020.

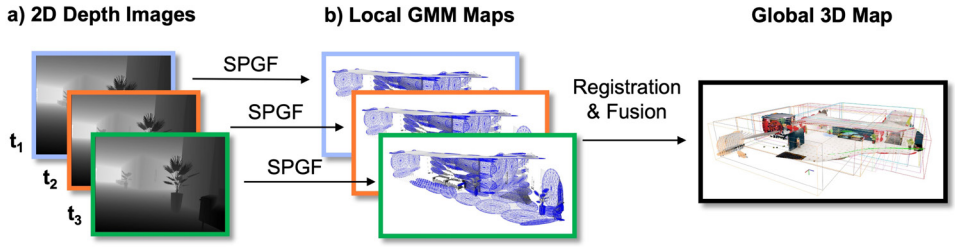
Memory-efficient Gaussian Fitting for Depth Images in Real Time

P. Z. X. Li, A. Wojtyna, S. Karaman, V. Sze
Sponsorship: NSF RTML 1937501, NSF CPS 1837212

We explore methods to enable motor systems to utilize sensor data to assess installation and detect or predict anomalous events before possible breakdown. Here, we use an autoencoder neural network model for unsupervised anomaly detection on an air-handling system driven by a switched-reluctance motor (Figure 1). The motor system consists of a belt-driven blower-motor unit with a 6/10 stator/rotor pole configuration.

Our model (Figure 2) takes the Fourier transform of recorded sensor time signals and trains one autoencoder per feature. The sum of the reconstruction errors is used as an anomaly score for prediction. The autoencoder has been effective on time series datasets in multiple fields. We generate datasets with differences in various parameters (e.g., belt tightness, motor speed, blower output valve condition) and label the data according to the anomalous scenarios. For instance, if a dataset is used for anomaly detection of belt tightness, we label the time series generated with normal belt tightness "normal" and an over tight/loose belt "anomalous." We choose three kinds of sensor data (line current, motor current, vibration) as the time series for anomaly detection. We assume that the system operates normally during training and that sensor data used for training purposes contain few, if any, anomalies.

The base frequencies of motor current and vibration are identical and consistent with the 6:10 pole ratio. Characteristic curves are found in randomly ordered runs for transient sensor data during activation (Figure 3). Results of stable sensor data show 100% area under curve (AUC) / 98% accuracy for anomaly detection of belt tightness, and 95% AUC / 82% accuracy for speed; 52% AUC / 34% accuracy for valve condition indicates that this condition remains difficult to detect. Combining the labels for the three parameters achieves 94% AUC / 87% accuracy. Our model detects anomalies on motor systems for one or several aggregated failure modes.



▲ Figure 1: (a) A depth image from a depth camera, and (b) a GMM (blue) generated using the proposed SPGF algorithm with a root-mean-square error of 9 cm, a memory overhead of 43 KB, a throughput of 32 fps, and an energy consumption of 0.11 J per frame using the low-power ARM Cortex-A57 CPU.

FURTHER READING

- P. Z. X. Li, S. Karaman, and V. Sze, "Memory-efficient Gaussian Fitting for Depth Images in Real Time," in *2022 International Conference on Robotics and Automation (ICRA)*. IEEE, 2022, pp. 8003–8009.

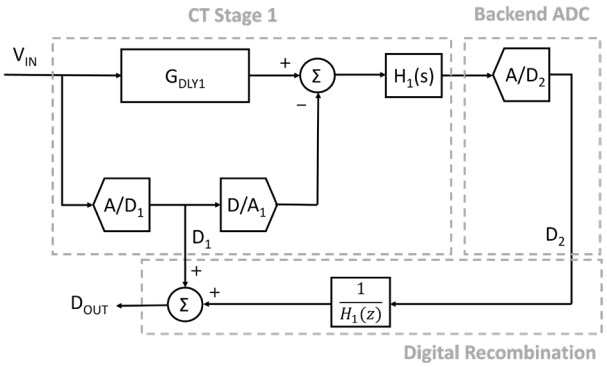
A Continuous-time Pipelined ADC with Time-interleaved Sub-ADC-DAC Path in 16-nm FinFET

R. Mittal, H. Shibata, S. Patil, E. Krommenhoek, P. Shrestha, G. Manganaro, A. P. Chandrakasan, H.-S. Lee
Sponsorship: Analog Devices Inc.

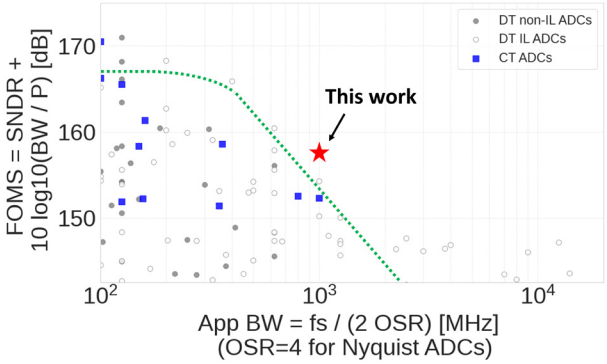
With the advent of the fifth-generation (5G) standard for cellular networks, direct radio frequency receivers are popular in applications such as cellular base stations. Such systems require analog-to-digital converters (ADC) with a high dynamic range over a large digitization bandwidth (> 500 MHz). For high-speed high-resolution ADCs with an upfront sampler, the clock jitter poses a fundamental bottleneck for the maximum achievable signal-to-noise ratio (SNR). In applications requiring 10-12 bit resolution for 1 GHz digitization bandwidth, the clock jitter values must be no more than a few tens of femtoseconds. This poses significant design challenges for the clock generator.

The continuous-time (CT) pipeline ADC is an emerging architecture that combines the benefits of a discrete-time pipeline ADC and a continuous-time ΔΣ ADC architecture. In this project, we explore the clock jitter sensitivity of the CT pipeline ADC. We derive the SNR limitations in a CT pipeline ADC and propose a new CT pipeline ADC design with improved tolerance to clock jitter. We also present a design methodology for the delay line and propose a novel inductor-less delay line that provides a good amplitude and phase matching between the stage 1 signal path and the sub-ADC-DAC path from DC to 1.6 GHz to minimize the signal leakage in the first stage residue.

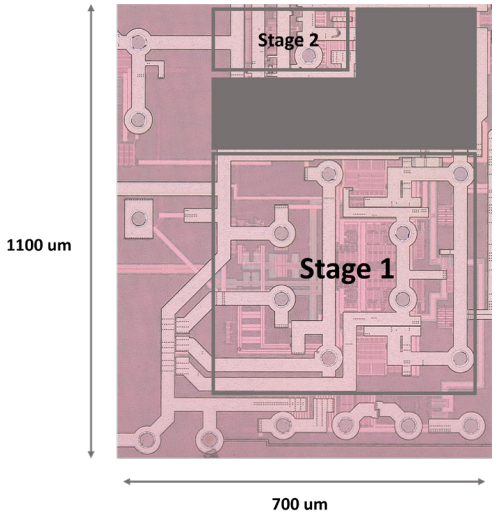
A prototype ADC was fabricated in 16-nm fin field-effect transistor process. The ADC achieves 61.7/60.8dB (low/high frequency) SNR over 1-GHz bandwidth. The active area is 0.77mm2 the ADC consumes 240mW. The Schreier figure-of-merit (FOM) is 157.9dB, which is among the best in comparison to other state-of-the-art continuous- time ADCs with digitization bandwidth greater than 500MHz.



▲ Figure 1: Block diagram of a 2-stage CT pipeline ADC. Stage 1 is a continuous-time stage, and stage 2 is a discrete-time ADC.



▲ Figure 2: Die photo of the prototype ADC. The ADC occupies 0.77mm2 and consumes 240mW power.



▲ Figure 3: FOMS vs. application bandwidth plot.

FURTHER READING

- B. Murmann, "ADC Performance Survey 1997-2022" [Online]. Available: *http://web.stanford.edu/~murmann/adcsurvey.html.*
- H. Shibata, et al. "16.2 A 9GS/s 1 GHz-BW Oversampled Continuous-time Pipeline ADC Achieving -161dBFS/Hz NSD." *2017 IEEE International Solid-State Circuits Conference* (ISSCC), IEEE, 2017.

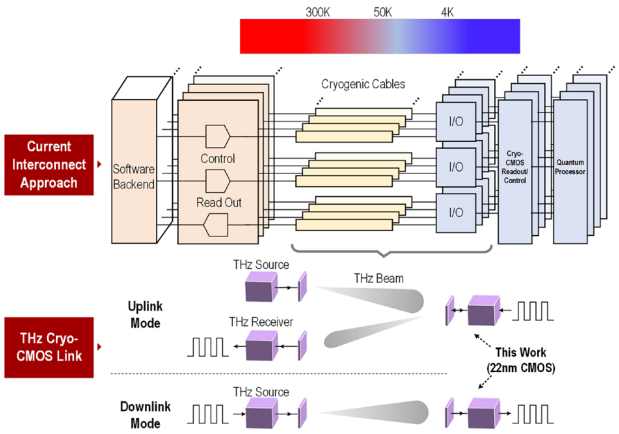
THz Cryo-CMOS Backscatter Transceiver: A Contactless 4 Kelvin-300 Kelvin Data Interface

J. Wang, M. I. Ibrahim, I. B. Harris, N. M. Monroe, M. I. W. Khan, X. Yi, D. R. Englund, R. Han
Sponsorship: Intel University Shuttle

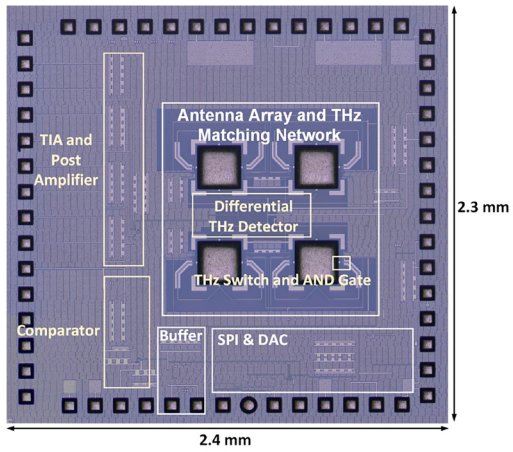
Modern low-temperature large-scale systems, such as high-sensitivity terahertz (THz) imaging arrays and quantum computers, require large-scale data interfaces between the cryogenic system core and room-temperature (RT) electronics. An error-protected quantum computer needs thousands or even millions of qubits operating at cryogenic temperature. However, its scalability is still largely limited by the cables connecting the quantum cores and peripheral control/processing units due to the heat load of cables. For example, a stainless-steel UT-085-SS-SS cable could pose close to one mW of heat load to the 4K stage, and tens of mW to the 50K stage in a dilution refrigerator. A 50-qubit quantum computer already has hundreds of cryogenic radio frequency (RF) cables, while the total power budget is limited to ~1W or even less.

In this project, we present a complementary metal-oxide semiconductor (CMOS) THz transceiver chip operating at 4K as a fully integrable alternative to the cryogenic RF cables. We determined an optimal carrier frequency of 260GHz based on the trade-off between the antenna dimension and the efficiency of the transistors. This frequency is sufficiently high to minimize the link footprint and to avoid potential disturbance of qubits, such as the superconducting or nitrogen-vacancy qubits, that typically operate at gigahertz; it also leads to much lower quantum noise (~ħω) compared to that in photonic links.

The transceiver avoids the power-hungry THz generation by using a passive backscatter communication scheme. A 4Gbps uplink is demonstrated with only 176fJ/b added heat load. In the downlink, we adopted a zero-power-consumption THz square-law detector. The receiver heat load is further reduced to 34fJ/b at 4.4Gbps. This fully contactless 4K-RT interface can be used to deliver digitized control/readout data, and even some analog/RF signals such as low phase noise clocks.



▲ Figure 1: Overview of the proposed contactless link replacing cryogenic cables in a cooled system.



▲ Figure 2: Die micrograph.

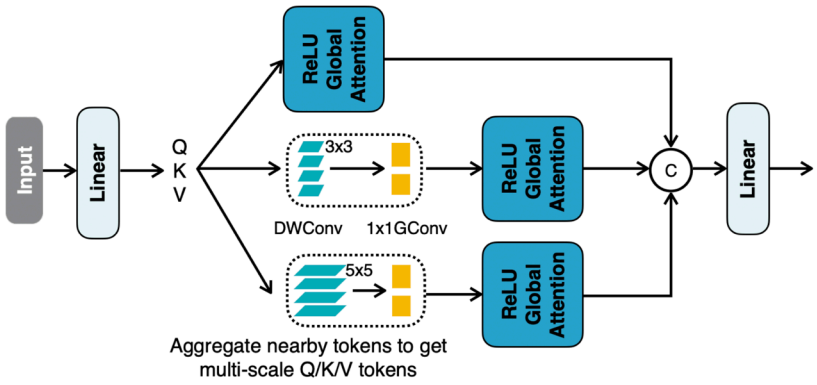
FURTHER READING

- J. Wang, M. I. Ibrahim, I. B. Harris, N. M. Monroe, M. I. W. Khan, X. Yi, D. R. Englund, and R. Han, "34.1 THz Cryo-CMOS Backscatter Transceiver: A Contactless 4 Kelvin-300 Kelvin Data Interface," *2023 IEEE International Solid- State Circuits Conference (ISSCC)*, pp. 504-506, 2023.

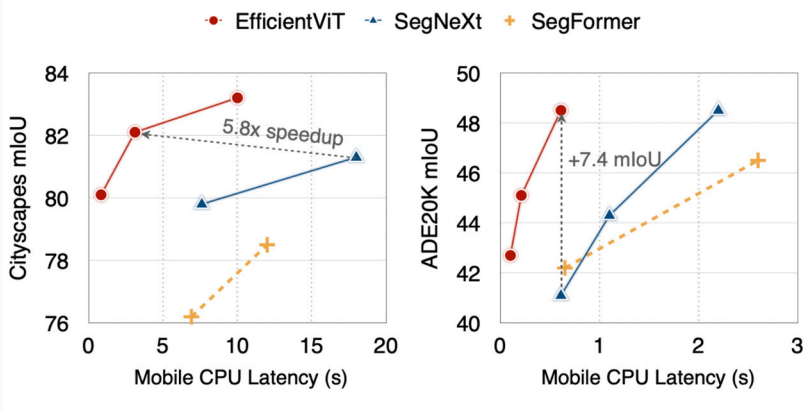
EfficientViT: Lightweight Multi-scale Attention for On-device Semantic Segmentation

H. Cai, J. Li, M. Hu, C. Gan, S. Han
Sponsorship: NSF, MIT-IBM Watson AI Lab, Ford, Intel, Qualcomm

Semantic segmentation enables many appealing real-world applications, such as computational photography, autonomous driving, etc. However, the vast computational cost makes deploying state-of-the-art semantic segmentation models on edge devices with limited hardware resources difficult. This work presents EfficientViT, a new family of semantic segmentation models with a novel lightweight multi-scale attention for on-device semantic segmentation. Unlike prior semantic segmentation models that rely on heavy self-attention, hardware-inefficient large-kernel convolution, or complicated topology structure to obtain good performances, our lightweight multi-scale attention achieves a global receptive field and multi-scale learning (two critical features for semantic segmentation models) with only lightweight and hardware-efficient operations. As such, EfficientViT delivers remarkable performance gains over previous state-of-the-art (SOTA) semantic segmentation models across popular benchmark datasets with significant speedup on the mobile platform. Without performance loss on Cityscapes, our EfficientViT provides up to 15x and 9.3x mobile latency reduction over SegFormer and SegNeXt, respectively. Maintaining the same mobile latency, EfficientViT provides +7.4 mIoU gain on ADE20K over SegNeXt.



◀ Figure 1: EfficientViT achieves a global receptive field and multi-scale learning with only efficient operations.



▶ Figure 2: EfficientViT provides significant performance boosts compared with prior state-of-the-art semantic segmentation models.

FURTHER READING

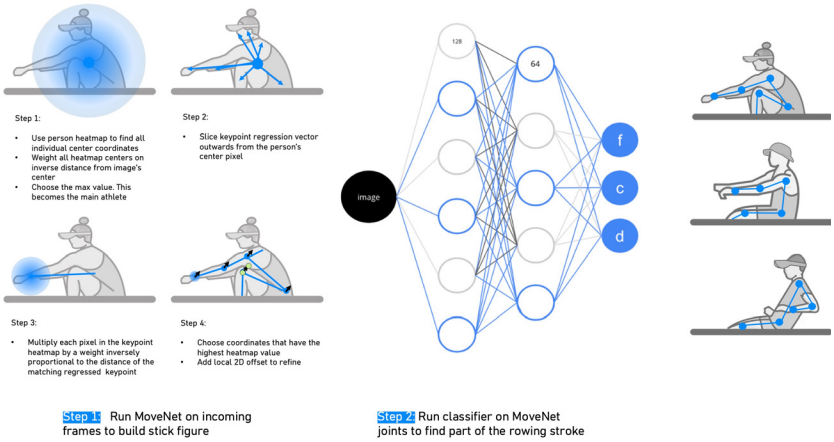
- Cai, Han, Li, Junyan, Hu, Muyan, Gan, Chuang, Han, Song, " EfficientViT: Lightweight Multi-scale Attention for On-device Semantic Segmentation," *arXiv preprint arXiv:2205.14756* (2022).

AI-Row: A Real-time Mobile ML Analytics Application for Para- and Non-para Rowers

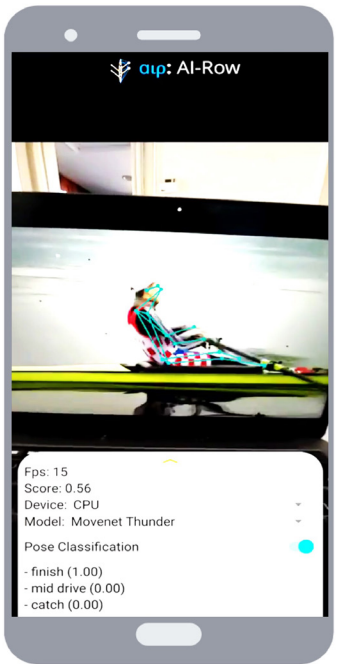
E. Eldracher, V. Muriga, S. Rodríguez, Y. Lin, Z. Liu, S. Han

Lightweight machine learning (ML) models can learn how to deliver elite rowing coaching to anyone, regardless of that individual's skill or physical ability. Despite the sport's predictability and angle-based technique, few tools exist to deliver data analytics on performance. Those that do are often expensive, not frequently optimized for both on-the-water and ergometer video, and trained without para inclusivity. This work harnesses the power of artificial intelligence to deliver technical insights in real time on a mobile device. This mobile application is the first use of mobile pose estimation ML for para-optimized rowing. It works for all athletes: those who use only their arms, those who use their arms and upper body, and those who use their legs, body, and arms.

By utilizing TensorFlow's MoveNet for mobile two-dimensional (2D) pose estimation combined with a simple classifier, we categorized three specific rowing poses both on the water and on the rowing machine. After locating an athlete's joints through MoveNet, our 26kb classifier predicts what part of the stroke a rower is in. At 18 frames/second, this classifier achieves around 89% accuracy. Because we built our own dataset of images (935 training, 235 testing, YouTube and USRowing images), this model is diverse and inclusive of both para and non-para athletes.



▲ Figure 1: Rendering of how our model predicts parts of the rowing stroke. Step 1 demonstrates MoveNet, Step 2 details our classifier, and the right-most side shows the three potential rowing positions categorized.



▲ Figure 2: Real-time screen recording of AI-Row. An android device correctly classifies a rower in the layback finish position.

FURTHER READING

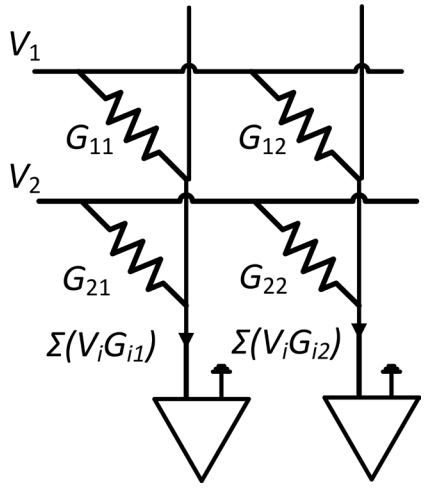
- R. Votel and N. Li, "Next-Generation Pose Detection with MoveNet and TensorFlow.js," *https://blog.tensorflow.org/2021/05/next-generation-pose-detection-with-movenet-and-tensorflowjs.html* (May 2021).
- Y. Wang, M. Li, H. Cai, W. Chen, and S. Han, "Lite pose: Efficient Architecture Design for 2D Human Pose Estimation," *Proc. IEEE/CVF Conference on Computer Vision and Pattern Recognition*, pp. 13126-13136, 2022.

ADCs for Analog Neural Nets

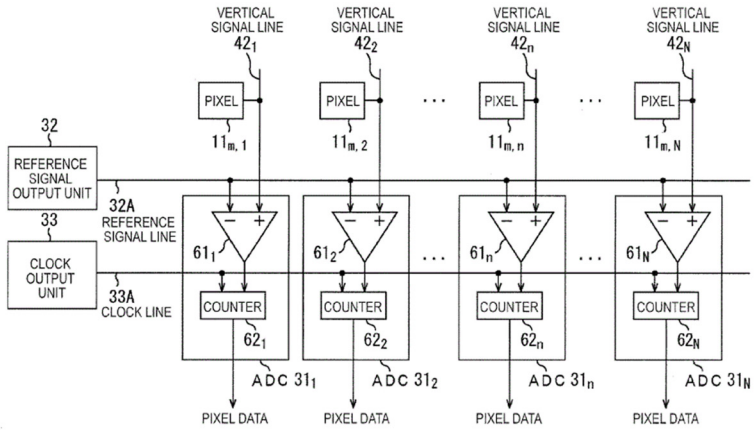
M. A. G. Elsheikh, H.-S. Lee
Sponsorship: MIT/MTL Samsung Semiconductor Research Fund

The meteoric rise of neural networks in recent years has been fueled by applications in several domains such as image recognition, self-driving cars, signal processing, and drug discovery. For more widespread deployment in portable applications, speed and power consumption must be improved. Employing specialized accelerator architectures offers improvements on both fronts. One accelerator topology, analog neural networks (ANNs), shown in Figure 1, perform matrix-vector-multiplications (MVMs) in the analog domain by encoding the inputs as the voltages and the weights as conductances. Summing up the currents in a common, virtual ground node is equivalent to performing the MVM process in one cycle, thereby potentially saving energy and time.

An analog-to-digital converter (ADC) architecture that is proposed for this application is the single slope ADC (SS-ADC), shown in Figure 2. The SS-ADC has become the standard architecture for complementary metal-oxide semiconductor (CMOS) image sensors as it is suitable for a medium number of bits, it is highly reconfigurable, and the peripheral circuits can fit the column pitch of the sensor elements. The column-parallel SS-ADC consists of a comparator and a counter for each column and a central ramp generator. At the beginning of the quantization process, the ramp and the counter are reset. The ramp starts increasing as the counter starts incrementing, and each column comparator compares between its analog column voltage and the ramp voltage. When the ramp value exceeds the column value, the comparator trips, and the counter value is held. This value is the digital representation of the column signal. In this research several innovations can be introduced to the SS-ADC to tailor it for ANNs to improve them beyond the state of the art in terms of speed and power consumption.



▲ Figure 1: Analog neural network accelerator.



▲ Figure 2: The column parallel architecture SS-ADC.

FURTHER READING

- Y. N. Wu, V. Sze and J. S. Emer, "An Architecture-Level Energy and Area Estimator for Processing-In-Memory Accelerator Designs," *2020 IEEE International Symposium on Performance Analysis of Systems and Software* (ISPASS), pp. 116-118, 2020.

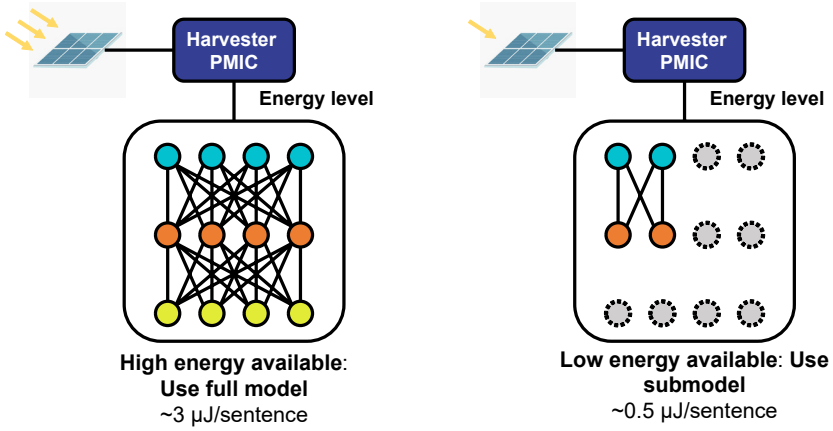
A Fully-integrated Energy-scalable Transformer Accelerator Supporting Adaptive Model Configuration and Word Elimination for Language Understanding on Edge Devices

A. Ji, H. Wang, M. Wang, S. Han, A. P. Chandrakasan
Sponsorship: TSMC

Efficient natural language processing (NLP) on the edge is needed to interpret voice commands, which have become an increasingly common way to interact with devices around us. Attention-based transformer models have replaced recurrent neural networks as the predominant model for NLP applications due to parallel input processing and the attention mechanism being able to capture both short and long-range relations. However, existing mainstream models (e.g., BERT, GPT) are way too large for edge devices. For simple NLP tasks on the edge, tiny custom transformer models can achieve good accuracy while being much more suitable for constrained hardware.

There are two main challenges when deploying lightweight NLP models on edge devices. Firstly, hardware constraints can fluctuate based on battery level, latency requirements, availability of compute resources, and accuracy tolerance. Adapting to these conditions typically requires multiple models of different sizes. For instance, when the device is less constrained, we may use a large model while under more constrained conditions, we may opt for a small model. But storing multiple models incurs a significant memory overhead. Secondly, sentences usually contain redundant words that contribute little to the overall understanding and may potentially be skipped during the majority of the processing. Conventional models spend an equal amount of time processing each word, leading to unnecessary computation.

Our work addresses these challenges with an energy-scalable transformer accelerator targeting small Internet of Things devices with two key features: 1) adaptive model configuration using a custom SuperTransformer model to generate models of various sizes while taking up only the memory footprint of a single full model; and 2) a comparator-based word elimination unit to progressively remove unimportant words from the sentence, reducing computation. We achieve 5.8× scalability in the network energy and latency. Word elimination can reduce network energy by 16% with some accuracy loss.



▲ Figure 1: Adaptive model configuration based on energy level of energy harvester using a single SuperTransformer model.

FURTHER READING

- H. Wang, Z. Zhang, and S. Han, "SpAtten: Efficient Sparse Architecture with Cascade Token Pruning and Head Pruning," *HPCA*, 2021.
- H. Wang, Z. Wu, Z. Liu, H. Cai, L. Zhu, C. Gan, and S. Han, "HAT: Hardware-Aware Transformers for Efficient Natural Language Processing," *ACL*, 2020.

LEGO: Spatial Accelerator Generation and Optimization for Tensor Applications

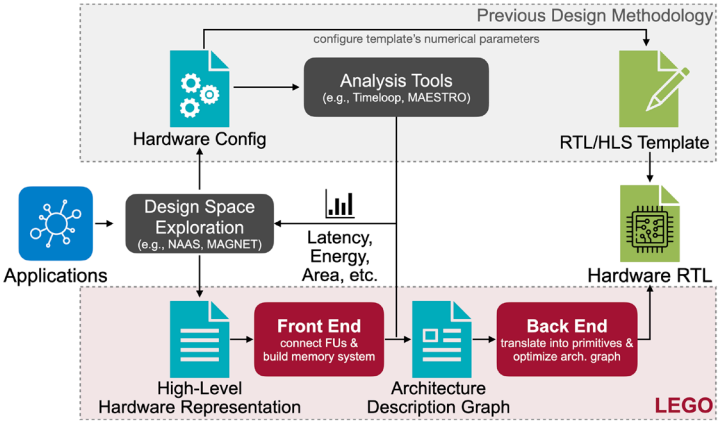
Y. Lin, Z. Zhang, S. Han
Sponsorship: SRC

The proliferation of tensor applications, such as deep neural networks, has led to an unprecedented demand for efficient and high-performing solutions. Particularly, modern foundation models and generative artificial intelligence (AI) applications require multiple input modalities (both vision and language), which increases the demand for flexible accelerator architecture. Existing frameworks suffer from the trade-off between design flexibility and productivity of register transfer language (RTL) generation: either limited to very few hand-written templates or unable to automatically generate the RTL.

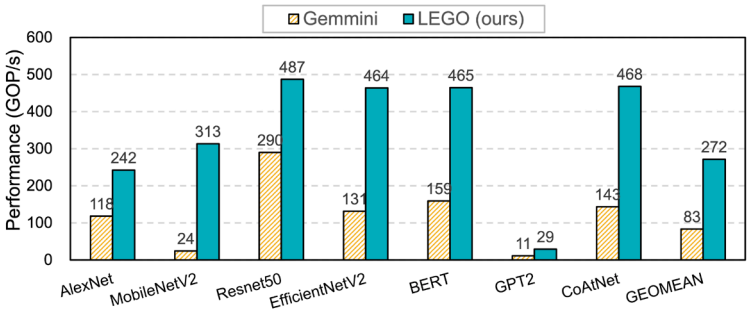
To address this challenge, we propose the LEGO framework, which automatically generates and optimizes spatial architecture design in the front end and outputs synthesizable RTL code in the back end without RTL templates. LEGO front end finds all possible interconnections between function units and determines the memory system shape by solving the integer linear equations and establishes the connections by a minimum-spanning-tree-based algorithm and a breadth-first-search-based heuristic algorithm for merging different spatial dataflow designs.

LEGO back end then translates the hardware in a primitive-level graph to perform lower-level optimizations and applies a set of linear-programming algorithms to optimally insert pipeline registers and reduce the overhead of unused logic when switching spatial dataflows.

Our evaluation demonstrates that LEGO can achieve 3.3× speedup and 2.1× energy efficiency compared to previous work by Gemmini and can generate one architecture for diverse modern foundation models in generative AI applications.



◀ Figure 1: Instead of configuring the sizing parameters in the hardware template, LEGO directly generates spatial architecture design and outputs RTL code from high-level hardware description.



▶ Figure 2: Performance comparison of Gemmini and LEGO. LEGO achieved an average 3.3× speedup over Gemmini. Both Gemmini and LEGO are bounded by memory bandwidth on GPT2. LEGO performs much better on MobileNetV2 due to its efficient support of depthwise convolution by dataflow switching.

FURTHER READING

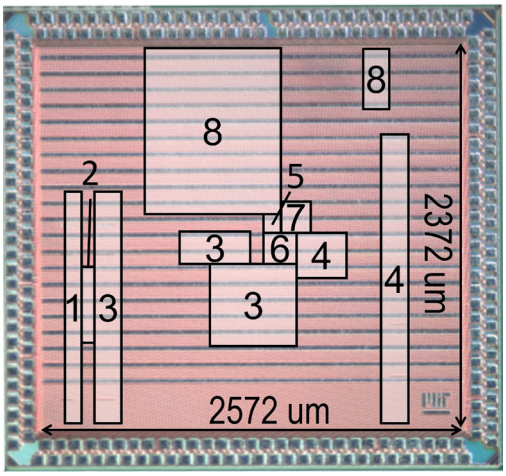
- Y. Lin, Z. Zhang, and S. Han, "LEGO: Spatial Accelerator Generation and Optimization for Tensor Applications," *https://naas.mit.edu.*
- H. Genc, S. Kim, A. Amid., A. Haj-Ali, V. Iyer, P. Prakash, J. Zhao, D. Grubb, H. Liew, H. Mao and A. Ou, "Gemmini: Enabling Systematic Deep-learning Architecture Evaluation via Full-stack Integration," *58th ACM/IEEE Design Automation Conference (DAC)* (pp. 769-774). IEEE, Dec. 2021.

Algorithm and Hardware Co-design for Efficient Video Understanding on the Edge

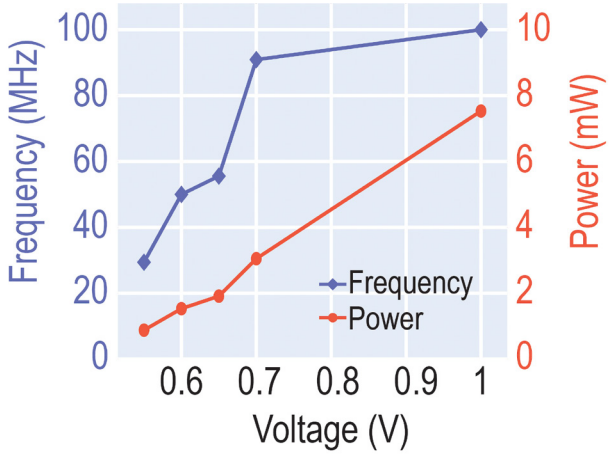
M. Wang, Y. Lin, Z. Zhang, J. Lin, S. Han, A. P. Chandrakasan
Sponsorship: Qualcomm Incorporated, TSMC University Shuttle Plan

With the rise of various applications including augmented reality/virtual reality, autonomous driving, object tracking for unmanned aerial vehicles, etc., there is an increasing need for accurate and energy-efficient video understanding on the edge. Although many deep learning chips are designed for images, little work has been done for videos. Video understanding on the edge has three major challenges. First, video understanding requires temporal modeling. For example, it identifies the difference between opening and closing a box, which is distinguishable only with temporal information considered. Second, many applications are delay-critical, such as self-driving cars and artificial intelligence drones. Third, high energy efficiency is important for edge devices with a tight power budget. Due to temporal continuity, consecutive frames might share a lot of common information, providing the potential to improve processing efficiency. However, an image-based processing system cannot utilize that since each frame is processed individually.

In this project, we co-design algorithms and hardware for energy-efficient video processing for delay-critical applications. We propose a real-time DiffFrame convolution achieving 2.2x dynamic random-access memory (DRAM) access reduction compared to conventional convolution at single-frame latency, design a sorter-free architecture for efficient utilization of temporal similarities between video frames, enable temporal modeling capability achieving high accuracy on video understanding applications, and optimize data buffering to remove DRAM traffic overhead for temporal modeling and reduce 55%--79% input activation DRAM traffic in depth-wise convolution layers. The chip consumes 40uJ/frame with 38 frames/second at 0.6V in 28nm TSMC 28-nm complementary metal-oxide-semiconductor (CMOS) process. Figure 1 shows the chip photograph; Figure 2 presents the frequency and power measurement results.Our demonstration of ferroelectricity in stacking-engineered TMD bilayers consolidates the feasibility of engineering 2D ferroelectric semiconductors and opens up a broad way of engineering various functional heterostructures out of non-ferroelectrics.



▲ Figure 1: Die micrograph (1: 16kB weight buffer; 2: 8x8 multiplier-and-accumulator array; 3: 32kB input activation buffer; 4: 44kB output activation and RefFrame unit; 5: DiffFrame generator; 6: DiffFrame pruning; 7: ConvMap buffer; 8: convolution map generator & coordinate buffer).

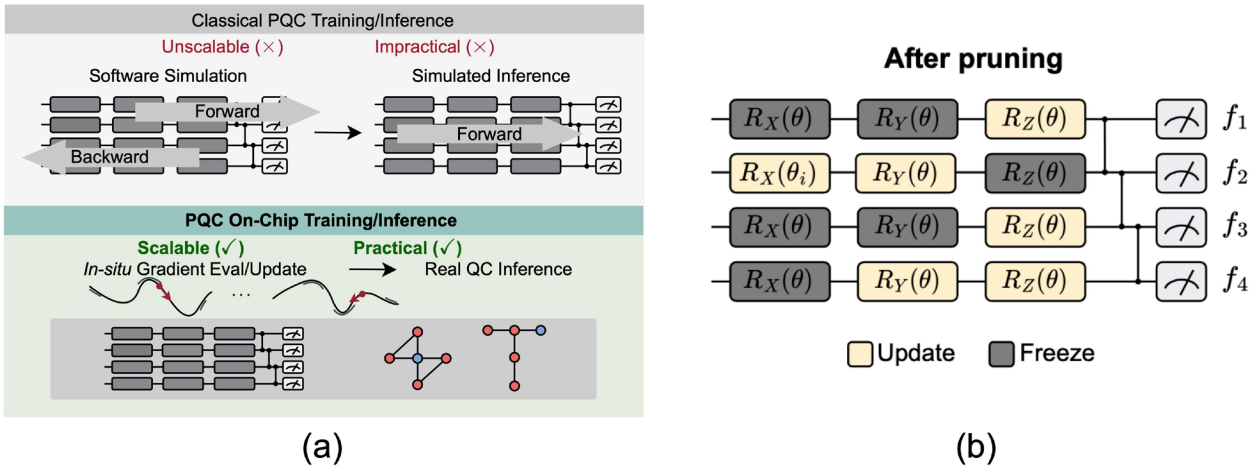


▲ Figure 2: Frequency and power measurements.

QOC: Quantum On-chip Training with Parameter Shift and Gradient Pruning

H. Wang, Z. Li, J. Gu, Y. Ding, D. Z. Pan, S. Han
Sponsorship: MIT-IBM Watson AI Lab, NSF CAREER Award, Qualcomm Innovation Fellowship

Parameterized quantum circuits (PQC) are drawing increasing research interest thanks to their potential to achieve quantum advantages on near-term noisy intermediate scale quantum (NISQ) hardware. In order to achieve scalable PQC learning, the training process needs to be offloaded to real quantum machines instead of using exponential-cost classical simulators. One common approach to obtain PQC gradients is parameter shift, whose cost scales linearly with the number of qubits. We present QOC, the first experimental demonstration of practical on-chip PQC training with parameter shift. Nevertheless, we find that due to the significant quantum errors (noises) on real machines, gradients obtained from naive parameter shift have low fidelity and thus degrade the training accuracy. To this end, we further propose probabilistic gradient pruning to first identify gradients with potentially large errors and then remove them. Specifically, small gradients have larger relative errors than large ones, thus having a higher probability to be pruned. We perform extensive experiments with the quantum neural network (QNN) benchmarks on 5 classification tasks using 5 real quantum machines. The results demonstrate that our on-chip training achieves over 90% and 60% accuracy for 2-class and 4-class image classification tasks, respectively. The probabilistic gradient pruning brings up to 7% PQC accuracy improvements over no pruning. Overall, we successfully obtain similar on-chip training accuracy compared with noise-free simulation but have much better training scalability. The QOC code is available in the TorchQuantum library.



▲ Figure 1: (a) In QOC, PQC training and inference are both performed on real quantum machines, making the whole pipeline scalable and practical. (b) Gradients are probabilistically pruned with a ratio in the pruning window to mitigate noises and stabilize training.

FURTHER READING

- H. Wang, Z. Li, J. Gu, Y. Ding, D. Z. Pan, and S. Han, "QOC: Quantum On-chip Training with Parameter Shift and Gradient Pruning," *Proc. 59th ACM/IEEE Design Automation Conference*, pp. 655-660, 2022.
- H. Wang, J. Gu, Y. Ding, Z. Li, F. T. Chong, D. Z. Pan, and S. Han, "QuantumNAT: Quantum Noise-aware Training with Noise Injection, Quantization and Normalization," in *Proc. 59th ACM/IEEE Design Automation Conference*, pp. 1-6, Jul. 2022.
- H. Wang, Y. Ding, J. Gu, Y. Lin, D. Z. Pan, F. T. Chong, and S. Han, "QuantumNAS: Noise-adaptive Search for Robust Quantum Circuits," *2022 IEEE International Symposium on High-Performance Computer Architecture* (HPCA), pp. 692-708, 2022.

Center for Integrated Circuits and Systems

Associate Professor Ruonan Han, Director

The Center for Integrated Circuits and Systems (CICS) at MIT, established in 1998, is an industrial consortium created to promote new research initiatives in circuits and systems design, as well as to promote a tighter technical relationship between MIT's research and relevant industry. Eight faculty members participate in the CICS: Director Ruonan Han, Hae-Seung (Harry) Lee, Anantha Chandrakasan, Song Han, David Perreault, Negar Reiskarimian, Charles Sodini, and Vivienne Sze.

CICS investigates circuits and systems for a wide range of applications, including artificial intelligence, wireless/wireline communication, sensing, security, biomedicine, power conversion, quantum information, among others.

We strongly believe in the synergistic relationship between industry and academia, especially in practical research areas of integrated circuits and systems. CICS is designed to be the conduit for such synergy.

CICS's research portfolio includes all research projects that the eight participating faculty members conduct, regardless of source(s) of funding, with a few exceptions.

Technical interaction between industry and MIT researchers occurs on both a broad and individual level. Since its inception, CICS recognized the importance of holding technical meetings to facilitate communication among MIT faculty, students, and industry. We hold two informal technical meetings per year open to CICS faculty, students, and representatives from participating companies. Throughout each full-day meeting, faculty and students present their research, often presenting early concepts, designs, and results that have not been published yet. The participants then offer valuable technical feedback, as well as suggestions for future research. The meeting also serves as a valuable networking event for both participants and students. Closer technical interaction between MIT researchers and industry takes place during work on projects of particular interest to participating companies. Companies may invite students to give on-site presentations, or they may offer students summer employment. Additionally, companies may send visiting scholars to MIT or enter into a separate research contract for more focused research for their particular interest. The result is truly synergistic, and it will have a lasting impact on the field of integrated circuits and systems.

Anantha P. Chandrakasan

Dean of Engineering, Vannevar Bush Professor of
Electrical Engineering & Computer Science
Department of Electrical Engineering and Computer Science

Design of digital integrated circuits and systems. Energy efficient implementation of signal processing, communication and medical systems. Circuit design with emerging technologies.

Rm. 38-107 | 617-258-7619 | anantha @ mit . edu

POSTDOCTORAL ASSOCIATE

Donghyeon Han, RLE
Yeseul Jeon, RLE

GRADUATE STUDENTS

Aya Amer, EECS Maitreyi Ashok, EECS
Ruicong Chen, EECS (co-supervised with H. Lee)
Adam Gierlach, EECS (co-supervised with G. Traverso)
Alex Ji, EECS
Mingran Jia, EECS (co-supervised with R. Han)
Dimple Kochar, EECS
Eunseok Lee, EECS (co-supervised with R. Han)
Kyungmi Lee, EECS
Mohith Harish Manohara, EECS
Saurav Maji, EECS
Rishabh Mittal, EECS (co-supervised with H-S. Lee)
Patricia Jastrzebska-Perfect (co-supervised with G. Traverso)
Zoey Song, EECS
Saebyeok Shin, EECS
Miaorong Wang, EECS
Jongchan Woo, EECS (co-supervised with Rabia T. Yazicigil)
So-Yoon Yang, EECS (co-supervised with G. Traverso)
Deniz Yildirim, EECS

VISITING SCHOLARS

Rabia Tugce Yazicigil, Boston University

SUPPORT STAFF

Katey Provost, Program/Project Coordinator

SELECTED PUBLICATIONS

A. Sahasrabudhe, L. E. Rupprecht, S. Orguc, T. Khudiyev, T. Tanaka, J. Sands, W. Zhu, A. Tabet, M. Manthey, H. Allen, G. Loke, M.-J. Antonini, D. Rosenfeld, J. Park, I. C. Garwood, W. Yan, F. Niroui, Y. Fink, A. Chandrakasan, D. V. Bohórquez, and P. Anikeeva, "Multifunctional Microelectronic Fibers Enable Wireless Modulation of Gut and Brain Neural Circuits," *Nature Biotechnology*, Jun. 2023.

M. Wang, Y. Lin, Z. Zhang, J. Lin, S. Han, and A. P. Chandrakasan, "VideoTime3: A 40uJ/frame 38FPS Video Understanding Accelerator with Real-Time DiffFrame Temporal Redundancy Reduction and Temporal Modeling," *IEEE Solid-State Circuits Letts.*, Jun. 2023.

J. Zhu, J.-H. Park, S. A. Vitale, W. Ge, G. S. Jung, J. Wang, M. Mohamed, T. Zhang, M. Ashok, M. Xue, X. Zheng, Z. Wang, J. Hansryd, A. P. Chandrakasan, J. Kong, and T. Palacios, "Low-thermal-budget Synthesis of Monolayer Molybdenum Disulfide for Silicon Back-end-of-line Integration on a 200mm Platform," *Nature Nanotechnology*, Apr. 2023.

R. Chen, A. Chandrakasan, and H.-S. Lee, "Sniff-SAR: A 9.8fJ/c.-s 12b Secure ADC with Detection-driven Protection against Power and EM Side-channel Attack," *IEEE Custom Integrated Circuit Conference (CICC)*, Apr. 2023.

E. Lee, M. I. W. Khan, X. Chen, U. Banerjee, N. Monroe, R. Yazicigil, R. Han, and A. Chandrakasan, "A 1.54mm2 Wake-Up Receiver Based on THz Carrier Wave and Integrated Cryptographic Authentication," *IEEE Custom Integrated Circuit Conference (CICC)*, Apr. 2023.

H. Sun, S. Maji, A. P. Chandrakasan, and B. Marelli, "Integrating Biopolymer Design with Physical Unclonable Functions for Anticounterfeiting and Product Traceability in Agriculture," *Science Advances*, Mar. 2023.

R. Agrawal, L. de Castro, G. Yang, C. Juvekar, R. Yazicigil, A. Chandrakasan, V. Vaikuntanathan, and A. Joshi, "FAB: An FPGA-based Accelerator for Bootstrappable Fully Homomorphic Encryption," *29th IEEE International Symposium on High-Performance Computer Architecture (HPCA)*, Feb. 2023.

M. R. Abdelhamid M. R., U. Ha, Utsav B., F. Adib, and A. P. Chandrakasan, "Batteryless, Wireless, and Secure SoC for Implantable Strain Sensing," *IEEE Open Journal of the Solid-State Circuits Society*, Dec. 2022.

S. Maji, U. Banerjee, S. H. Fuller, and A. P. Chandrakasan, "A ThreshoId-ImpIementation-Based Neural-Network Accelerator Securing Model Parameters and Inputs Against Power Side-Channel Attacks," *IEEE Journal of Solid-State Circuits*, Nov. 2022.

Q. Liu, M. Jimenez, M. E. Inda, A. Riaz, T. Zirtiloglu, A. Chandrakasan, T. K. Lu, G. Traverso, P. Nadeau, and R. T. Yazicigil, "A Threshold-based Bioluminescence Detector with a CMOS-Integrated Photodiode Array in 65nm for a Multi-Diagnostic Ingestible Capsule," *IEEE Journal of Solid-State Circuits*, Aug. 2022.

Ruonan Han

Director of Center for Integrated Circuits and Systems
Associate Professor of Electrical Engineering & Computer Science
Officer of the Electrical Engineering & Computer Science Undergraduate Laboratory
Department of Electrical Engineering & Computer Science

Integrated circuits and systems operating from RF to THz frequencies for sensing and communication applications. Electromagnetism, Chip-scale wave-matter interactions for miniature spectroscopy and frequency metrology.

Rm. 39-527A | 617-324-5281 | ruonan @ mit . edu

GRADUATE STUDENTS

Cole Brabec (Co-supervised with Dirk Englund), EECS
Xibi Chen, EECS
Mingran Jia (Co-supervised with Anantha Chandrakasan), EECS
Eunseok Lee (Co-supervised with Anantha Chandrakasan), EECS
Jinchen Wang, EECS

SUPPORT STAFF

Kathleen Brody, Administrative Assistant
Elizabeth Kubicki, Administrative Assistant

SELECTED PUBLICATIONS

M. ElKabbash, I. Harris, S. Trajtenberg-Mills, S. Bandyopadhyay, X. Chen, M. Ibrahim, R. Han, and D. Englund, "Zero-change CMOS Nanophotonics: Converting Foundry CMOS Chips to Plasmonic Electro-optic Modulators," *Conf. on Lasers and Electro-Optics (CLEO)*, San Jose, CA, May 2023.

E. Lee, M. I. W. Khan, X. Chen, U. Banerjee, N. Monroe, R. Yazicigil, R. Han, and A. Chandrakasan, "A 1.54mm^2 Wake-Up Receiver Based on THz Carrier Wave and Integrated Cryptographic Authentication," *IEEE Custom Integrated Circuit Conf. (CICC)*, San Antonio, TX, Apr. 2023.

K. K. O, W. Choi, and R. Han, "Perspective on Active Submillimeter Electromagnetic Wave Imaging Using CMOS Integrated Circuits Technologies," *J. of Applied Physics*, vol. 133, no. 15, Apr. 2023.

J. Wang, M. I. Ibrahim, I. B. Harris, N. M. Monroe, M. I. W. Khan, X. Yi, D. R. Englund, and R. Han, "THz Cryo-CMOS Backscatter Transceiver: A Contactless 4 Kelvin-300 Kelvin Data Interface," *IEEE Intl. Solid-State Circuit Conf. (ISSCC)*, San Francisco, CA, Feb. 2023.

X. Chen, X. Yi, M. Khan, X. Li, W. Chen, J. Zhu, Y. Yang, K. Kolodziej, N. Monroe, and R. Han, "A 140-GHz FMCW TX/RX-Antenna-Sharing Transceiver with Low-Inherent-Loss Duplexing and Adaptive Self-Interference Cancellation," *IEEE Journal of Solid-State Circuits (JSSC)*, vol. 57, no. 12, Dec. 2022.

X. Li, W. Chen, H. Wu, S. Li, X. Yi, R. Han and Z. Feng, "A 110-to-130 GHz SiGe BiCMOS Doherty Power Amplifier with A Slotline-Based Power Combiner," *IEEE J. of Solid-State Circuits (JSSC)*, vol. 57, no. 12, Dec. 2022.

J. Woo, M. Khan, M. Ibrahim, R. Han, A. Chandrakasan, and R. Yazicigil, "Physical-Layer Security for THz Communications via Orbital Angular Momentum Waves," *2022 IEEE International Workshop on Signal Processing Systems (SiPS)*, Rennes, France, Nov. 2022.

A. Yen, M. Kim, L. Yi, H. Javadi, and R. Han, "Integrable Timing on Silicon Wafer Supporting CubeSats-Based Communications, Navigation and Radio Science," *AIAA Accelerating Space Commerce, Exploration, and New Discovery (ASCEND)*, Las Vegas, NV, Oct. 2022.

M. I. W. Khan, E. Lee, N. Monroe, A. Chandrakasan, and R. Han, "A Dual-Antenna, 263GHz Energy Harvester in CMOS for Ultra-Miniaturized Platforms with 13.6% RF-to-DC Conversion Efficiency at -8dBm Input Power," *IEEE Radio-Frequency Integrated Circuit Symposium (RFIC)*, Denver, CO, Jun. 2022.

M. Kim, C. Wang, L. Yi, H. Lee, and R. Han, "A Sub-THz CMOS Molecular Clock with 20 ppt Stability at 10,000 s Based on A Dual-Loop Spectroscopic Detection and Digital Frequency Error Integration," *IEEE Radio-Frequency Integrated Circuit Symposium (RFIC)*, Denver, CO, Jun. 2022.

Q. Yu, G. Kim, J. Garrett, D. Thomson, G. Dogiamis, N. M. Monroe, R. Han, Y. Ma, J. Waldemer, Y. S. Nam, G. Beltran, V. Neeli, S. Ravikumar, S. Rami, C. Pelto, and E. Karl, "Low-Loss On-Chip Passive Circuits Using C4 Layer for RF, mmWave and sub-THz Applications," *IEEE International Microwave Symposium (IMS)*, Denver, CO, Jun. 2022.

M. I. W. Khan, J. Woo, X. Yi, M. I. Ibrahim, R. T. Yazicigil, A. P. Chandrakasan, and R. Han, "A 0.31-THz Orbital-Angular-Momentum (OAM) Wave Transceiver in CMOS With Bits-to-OAM Mode Mapping," *IEEE J. of Solid-State Circuits*, vol. 57, no. 5, pp. 1344-1357, May 2022.

L. Li, L. de Santis, I. Harris, K. Chen, Y. Song, I. Christen, M. Trusheim, C. Herranz, R. Han, and D. Englund, "Scalable Quantum Information Processing Architecture Using A Programmable Array of Spin-Photon Interfaces," *Conf. on Lasers and Electro-Optics (CLEO)*, San Jose, CA, May 2022.

Song Han

Associate Professor
Department of Electrical Engineering & Computer Science

Machine learning, artificial intelligence, model compression, hardware acceleration

Rm. 38-344 | 617-253-0086 | songhan @ mit . edu

POSTDOCTORAL ASSOCIATES

Wei-Ming Chen, EECS
Wei-Chen Wang, EECS

GRADUATE STUDENTS

Han Cai, EECS
Qiyao (Catherine) Liang, EECS
Ji Lin, EECS
Yujun Lin, EECS
Zhijian Liu, EECS
Haotian Tang, EECS
Hanrui Wang, EECS
Guangxuan Xiao, EECS
Zhekai Zhang, EECS
Ligeng Zhu, EECS

UNDERGRADUATE STUDENTS

Emelie Eldracher, EECS
Kevin Shao, EECS

SUPPORT STAFF

Jami L. Mitchell, Administrative Assistant

SELECTED PUBLICATIONS

G. Xiao, J. Lin, M. Seznec, H. Wu, J. Demouth, and S. Han, "SmoothQuant: Accurate and Efficient Post-Training Quantization for Large Language Models," *International Conference on Machine Learning (ICML)*, 2023.

Z. Liu, X. Yang, H. Tang, S. Yang, and S. Han, "FlatFormer: Flattened Window Attention for Efficient Point Cloud Transformer," *Computer Vision and Pattern Recognition Conference (CVPR)*, 2023.

X. Chen*, Z. Liu*, H. Tang, L. Yi, H. Zhao, and S. Han, "SparseViT: Revisiting Activation Sparsity for Efficient High-Resolution Vision Transformer," *Computer Vision and Pattern Recognition Conference (CVPR)*, 2023.

Z. Liu*, H. Tang*, A. Amini, X. Yang, H. Mao, D. L. Rus, and S. Han, "BEVFusion: Multi-Task Multi-Sensor Fusion with Unified Bird's-Eye View Representation," *International Conference on Robotics and Automation (ICRA)*, 2023.

J. Lin*, L. Zhu*, W. Chen, W. Wang, C. Gan, and S. Han, "On-Device Training Under 256KB Memory," *Neural Information Processing System (NeurIPS)*, 2022.

M. Li, J. Lin, C. Meng, S. Ermon, S. Han, and J. Zhu, "Efficient Spatially Sparse Inference For Conditional Gans And Diffusion Models," *Neural Information Processing System (NeurIPS)*, 2022.

Y. Wang, M. Li, H. Cai, W. Chen, and S. Han, "LitePose: Efficient Architecture Design for 2D Human Pose Estimation," *Computer Vision and Pattern Recognition Conference (CVPR)*, 2022.

H. Cai, J. Lin, Y. Lin, Z. Liu, H. Tang, H. Wang, L. Zhu, and S. Han, "Enable Deep Learning on Mobile Devices: Methods, Systems, and Applications," *Transactions on Design Automation of Electronic Systems (TODAES)*, 2022.

H. Cai, C. Gan, J. Lin, and S. Han, "Network Augmentation for Tiny Deep Learning," *International Conference on Learning Representations (ICLR)*, 2022.

H. Tang, Z. Liu, X. Li, Y. Lin, and S. Han, "TorchSparse: Efficient Point Cloud Inference Engine," *Conference on Machine Learning and Systems (MLSys)*, 2022.

H. Wang, Y. Ding, J. Gu, Z. Li, Y. Lin, D. Pan, F. Chong, and S. Han, "QuantumNAS: Noise-Adaptive Search for Robust Quantum Circuits," *International Symposium on High-Performance Computer Architecture (HPCA)* 2022

H. Wang, Z. Li, J. Gu, Y. Ding, D. Z. Pan, and S. Han, "QOC: Quantum On-Chip Training with Parameter Shift and Gradient Pruning," *Design Automation Conference (DAC)*, 2022.

H. Wang, J. Gu, Y. Ding, Z. Li, F. T. Chong, D. Z. Pan, and S. Han, "QuantumNAT: Quantum Noise-Aware Training with Noise Injection, Quantization and Normalization," *Design Automation Conference (DAC)*, 2022.

Hae-Seung Lee

ATSC Professor of Electrical Engineering & Computer Science
Department of Electrical Engineering & Computer Science

Analog and Mixed-signal Integrated Circuits, with a Particular Emphasis in Data Conversion Circuits in scaled CMOS.

Rm. 39-521 | 617-253-5174 | hslee @ mtl . mit . edu

POSTDOCTORAL ASSOCIATE

Anand Chandrasekhar, EECS

GRADUATE STUDENTS

Ruicong Chen, EECS
Mohamed Elsheikh, EECS
Rebecca Ho, EECS
Jaehwan Kim, EECS
Rishabh Mittal, EECS

SUPPORT STAFF

Elizabeth Kubicki, Administrative Assistant

PUBLICATIONS

A. Chandrasekhar, R. Padrós-Valls, R. Pallaròs-Lopéz, E. Palanques-Tost, N. Houstis, T. M. Sundt, H.-S. Lee, C. G. Sodini, and A. D. Aquirre, "Tissue Perfusion Pressure Enables Continuous Hemodynamic Evaluation and Risk Prediction in the Intensive C are Unit," *Nature Medicine* 29, Aug. 2023, https://doi.org/10.1038/s41591-023-02474-6.

R. Chen, A. P. Chandrakasan, and H.-S. Lee, "RaM-SAR: A Low Energy and Area Overhead, 11.3fJ/conv.-step. 12b 25MS/s Secure Random-mapping SAR ADC with Power and EM Side-channel Attack Protection," *2022 IEEE Symposium on VLIS Circuits*, Jun. 12-17, 2022, Hawaii, HI.

M. Kim, C. Wang, L. Yi, H.-S. Lee, and R. Han, "A Sub-THz CMOS Molecular Clock with 20 ppt Stability at 10,000 s Based on A Dual-Loop Spectroscopic Detection and Digital Frequency Error Integration," *2022 IEEE RFIC*, Jun. 19-21, 2022, Denver, CO.

R. Chen, H. T. Kung, A. P. Chandrakasan, and H.-S. Lee, "A Bit-level Sparsity-aware SAR ADC with Direct Hybrid Encoding for Signed Expressions for AIoT Applications," *2022 IEEE/ACM International Symposium on Low Power Electronics and Design*, Aug. 1-2, 2022, Boston, MA.

R. Chen, A. P. Chandrakasan, and H.-S. Lee, "Sniff-SAR: A 9.8fJ/c.-s 12b Secure ADC with Detection-driven Protection Against Power and EM Side-channel Attack," *2023 IEEE Custom Integrated Circuits Conference*, Apr. 23-26, 2023, San Antonio, TX.

R. Mittal, H. Shibata, S. Patil, E. Krommenhoek, P. Shrestha, G. Manganaro, A. P. Chandrakasan, and H.-S. Lee, "A 6.4GS/s 1-GHz BW Continuous-time Pipelined ADC with Time-interleaved Sub-ADC-DAC Achieving 61.7-dB SNDR in 16-nm FinFET," *2023 IEEE Symposium on VLIS Circuits*, Jun. 11-16, 2023, Kyoto, Japan.

J. Zheng, H. Wang, A. Chandrasekhar, A. Aguirre, S. Han, H.-S. Lee, and C. G. Sodini, "Machine Learning for Arterial Blood Pressure Predtion," *2023 Conference on Health, Inference, and Learning*, Jun. 22-23, 2023, Cambridge, MA.

H.-S. Lee, "Multipath Sampling Circuits," U.S. Patent 11,533,060, Dec. 20, 2022.

David Perreault

Ford Professor of Engineering
Department of Electrical Engineering & Computer Science

Power electronics and energy conversion systems, high-efficiency radio-frequency power amplifiers and rf applications, Renewable energy systems, applications of power electronics in industrial, commercial, scientific, transportation, and biomedical systems

Rm. 10-172 | (617) 258-6038 | djperrea @ mit . edu

POSTDOCTORAL ASSOCIATE

Xin Zan, RLE

GRADUATE STUDENTS

Julia Estrin, EECS
K Rafa Islam, EECS
Amanda Jackson, EECS
Mansi Joisher, EECS
Mohammad Qasim, EECS
Rachel Yang, EECS

UNDERGRADUATE STUDENTS

Sarah Coston, EECS

SUPPORT STAFF

David M. Otten, Prinicipal Research Engineer
Donna Gale, Administrative Assistant

SELECTED PUBLICATIONS

J. G. Kassakian, D.J. Perreault, G. C. Verghese, and M. F. Schlecht, "Principles of Power Electronics," *2nd ed. Cambridge: Cambridge University Press*, 2023.

J. D. Boles, J. E. Bonavia, J. H. Lang, and D.J. Perreault, "A Piezoelectric-Resonator-Based DC-DC Converter Demonstrating 1 kW/cm Resonator Power Density," I*EEE Transactions on Power Electronics*, vol. 38, no. 8, pp. 10012-10025, Aug. 2023.

H. Andersen, Y. Chen, M. M. Qasim, D. G. Guadrado, D.M. Otten, E. Greitzer, D.J. Perreault, J.L. Kirtley, J.H. Lang and Z. Spakovsky, "Design and Manufacturing of a High-Specific-Power Electric Machine for Aircraft Propulsion," *AIAA/IEEE Electric Aircraft Technologies Symposium (EATS)*, Jun. 2023.

X. Zan, K. N. R. Islam, and D. J. Perreault, "Wide-Range Switched-Mode Power Amplifier Architecture," *2023 IEEE Workshop on Control and Modeling for Power Electronics*, Jun. 2023.

E. Ng, J. D. Boles, J. H. Lang and D. J. Perreault, "Piezoelectric Transformer Component Design for DC-DC Power Conversion," *2023 IEEE Workshop on Control and Modeling for Power Electronics,* Jun. 2023.

Y. Chen, Z. S. Spakovsky, E. M. Greitzer, Z. C. Cordero, J. H. Lang, J. L. Kirtley, D. J. Perreault, H. N. Andersen, M. M. Qasim, D. G. Cuadrado, and D. M. Otten, "Technology Demonstration of a Megawatt-Class Integrated Motor Drive for Aircraft Propulsion," *AIAA/IEEE Electric Aircraft Technologies Symposium (EATS)*, Jun. 2023.

M. M. Qasim, D. M. Otten, Z. S. Spakovszky, J. H. Lang, J. L. Kirtley, and D. J. Perreault, "Design and Optimization of an Inverter for a One-Megawatt Ultra-Light Motor Drive," *AIAA/IEEE Electric Aircraft Technologies Symposium (EATS)*, Jun. 2023.

Z. Shen, W. Chen, H. Zhao, L. Jin, A.J. Hanson, D. J. Perreault, C.R. Sullivan, F. Blaabjerg, and H. Wang, "Core Energy Capacitance of NiZn Inductors," *IEEE Transactions on Power Electronics*, Vol 8, No. 4, pp. 4235-4240, Apr. 2023.

M. K. Ranjram and D. J. Perreault, "A Modeling Approach for the VIRT and Other Coupled Electronic and Magnetic Systems," *IEEE Journal of Emerging and Selected Topics in Power Electronics,* Vol. 10, No. 6, pp. 6728-6741, Dec. 2022.

J. D. Boles, E. Ng, J. H. Lang, and D. J. Perreault, "DC-DC Converter Implementations Based on Piezoelectric Transformers," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, Vol. 10, No. 6, pp. 6754-6769, Jun. 2022.

R. S. Yang, A. B. Nadler, C. R. Sullivan and D. J. Perreault, "Permanent Magnet Hybrid Core Inductors for High Saturation Capability," *2022 IEEE Workshop on Modeling and Control in Power Electronics*, Jun. 2022.

J. D. Boles, J. J. Piel, E. Ng, J. E. Bonavia, B. M. Wanyeki, J. H. Lang and D. J. Perreault, "Opportunities, Progress and Challenges in Piezoelectric-Based Power Electronics," *2022 International Power Electronics Conference*, May 2022, invited.

J. D. Boles, J. J. Piel, E. Ng, J. E. Bonavia, J. H. Lang and D. J. Perreault, "Piezoelectric-Based Power Conversion: Recent Progress, Opportunities and Challenges," *2022 IEEE Custom Integrated Circuits Conference*, Apr. 2022, invited.

H. Zhang, G. Cassidy, A. Jurkov, K. Luu, A. Radomski, and D. J. Perreault, "Modeling and Design of High-Power Non-Isolating RF Power Combiners Based on Transmission Lines," *2022 IEEE Applied Power Electronics Conference,* Mar. 2022.

Negar Reiskarimian

X-Window Consortium Career Development Assistant Professor
Department of Electrical Engineering & Computer Science

Integrated circuits and systems and applied electromagnetics with a focus on analog, RF, millimeter-Wave (mm-Wave) and optical integrated circuits, metamaterials and systems for a variety of applications.

Rm. 39-427a | 617-253-0726 | negarr @ mit . edu

GRADUATE STUDENTS

Soroush Araei, EECS
Shahabeddin Mohin, EECS
Sarina Sabouri, EECS, MIT Analog Devices Fellow
(co-supervised with A. Chandrakasan)
Melania St. Cyr, EECS, Draper Fellow
Haibo Yang, EECS, MIT Jacobs Fellow

UNDERGRADUATE STUDENTS

Deniz Erus, UROP

SUPPORT STAFF

Maria Markulis, Administrative Assistant

SELECTED PUBLICATIONS

S. Araei, S. Mohin, and N. Reiskarimian, "Realization of Low-Loss Fully-Passive Harmonic Rejection N-Path Filters," *IEEE International Microwave Symposium (IMS)*, Jun. 2023 [invited and to appear in *IEEE Microwave and Wireless Technology Letters (MWTL)*].

S. Araei, S. Mohin, and N. Reiskarimian, "An Interferer-Tolerant Harmonic-Resilient Receiver with >+10dBm 3rd Harmonic Blocker P1dB for 5G NR Applications," in *IEEE International Solid-State Circuits Conference (ISSCC)*, pp. 294-295, Feb. 2023.

N. Reiskarimian, "A Review of Nonmagnetic Nonreciprocal Electronic Devices: Recent Advances in Nonmagnetic Nonreciprocal Components," *IEEE Solid-State Circuits Magazine* vol. 13, no. 4, pp. 112-121, Fall 2021.

N. Reiskarimian, M. Khorshidian, and H. Krishnaswamy, "Inductorless, Widely Tunable N-Path Shekel Circulators-Based on Harmonic Engineering," *IEEE J. of Solid-State Circuits (JSSC)* (invited), vol. 56, no. 4, Apr. 2021.

A. Nagulu, N. Reiskarimian, and H. Krishnaswamy, "Non-reciprocal Electronics Based on Temporal Modulation," *Nature Electronics*, May 2020.

M. Khorshidian, N. Reiskarimian, and H. Krishnaswamy, "A Compact Reconfigurable N-Path Low-Pass Filter Based on Negative Trans-Resistance with <1dB Loss and >21dB Out-of-Band Rejection," in *IEEE International Microwave Symposium (IMS)*, pp. 799-802, Jun. 2020.

M. Khorshidian, N. Reiskarimian and H. Krishnaswamy, "High-Performance Isolators and Notch Filters based on N-Path Negative Trans-Resistance," in *IEEE International Solid-State Circuits Conference (ISSCC)*, Feb. 2020.

M. Baraani Dastjerdi, S. Jain, N. Reiskarimian, A. Natarajan and H. Krishnaswamy, "Analysis and Design of Full-Duplex 2x2 MIMO Circulator-Receiver with High TX power handling Exploiting MIMO RF and Shared-de- lay Baseband Self-Interference Cancellation," *IEEE J. of Solid-State Circuits (JSSC)* (invited), vol. 54, no. 12, pp. 3525-3540, Dec. 2019.

N. Reiskarimian, M. Tymchenko, A. Alu and H. Krishnaswamy, "Breaking Time-Reversal Symmetry Within Infinitesimal Dimensions Through Staggered Switched Networks," in *Metamaterials*, Sep. 2019.

N. Reiskarimian, A. Nagulu, T. Dinc and H. Krishnaswamy, "Non-Reciprocal Devices: A Hypothesis Turned into Reality," *IEEE Microwave Magazine* (invited), vol. 20, no. 4, pp. 94-111, Apr. 2019.

Charles G. Sodini

LeBel Professor
Department of Electrical Engineering & Computer Science

Electronics and integrated circuit design and technology. Specifically, his research involves technology intensive integrated circuit and systems design, with application toward medical electronic devices for personal monitoring of clinically relevant physiological signals.

Rm. 39-527b | 617-253-4938 | sodini @ mtl . mit . edu

COLLABORATORS

Sam Fuller, Analog Devices, Inc
Joohyun Seo, Analog Devices, Inc.

POSTDOCTORAL ASSOCIATE

Anand Chandrasekhar, MTL

SUPPORT STAFF

Kathleen Brody, Administrative Assistant

SELECTED PUBLICATIONS

H.-Y. Lai, C. G. Sodini, T. Heldt, and V. Sze, "Individualized Tracking of Neurocognitive-state-dependent Eye-movement Features Using Mobile Devices," accepted for publication in *Proceedings of the ACM on Interactive, Mobile, Wearable and Ubiquitous Technologies* 7(1):1-23, 2023.

S. M. Imaduddin, C. G. Sodini, and T. Heldt, "Deconvolution-based Partial Volume Correction for Volumetric Blood Flow Measurement," *IEEE Transactions on Ultrasonics, Ferroelectrics, and Frequency Control*, 69(8): 2484-2498, Apr. 2022.

J. Seo, H.-S. Lee, and C. G. Sodini, "Non-Invasive Evaluation of a Carotid Arterial Pressure Waveform Using Motion-Tolerant Ultrasound Measurements During the Valsalva Maneuver," *IEEE J. of Biomedical and Health Informatics*, vol. 25, no. 1, Jan. 2021.

H.-Y. Lai, G. Saavedra-Peña, C. G. Sodini, V. Sze, and T. Heldt, "App-based Saccade Latency and Error Determination Across the Adult Age Spectrum," *IEEE Transactions on Biomedical Engineering* 69(2): 1029-1039, 2021.

H.-Y. Lai, G. Saavedra-Peña, C. G. Sodini, V. Sze, and T. Heldt, "Measuring Saccade Latency Using Smartphone Cameras," *IEEE J. of Biomedical and Health Informatics*, vol. 24, no. 3, pp. 885-897, Mar. 2020.

Vivienne Sze

Associate Professor of Electrical Engineering & Computer Science
Department of Electrical Engineering & Computer Science

Joint design of signal processing algorithms, architectures, VLSI and systems for energy-efficient implementations. Applications include computer vision, machine learning, autonomous navigation, image processing and video coding.

Rm. 38-260 | 617-324-7352 | sze @ mit . edu

GRADUATE STUDENTS

Tanner Andrulis, EECS (co-advised with Joel Emer)
Zih-Sing Fu, EECS (co-advised with Sertac Karaman)
Dasong Gao, EECS (co-advised with Sertac Karaman)
Keshav Gupta, EECS (co-advised with Sertac Karaman)
Jamie Koerner, EECS (co-advised with Thomas Heldt)
Peter Li, EECS (co-advised with Sertac Karaman)
Soumya Sudhakar, AeroAstro (co-advised with Sertac Karaman)
Yannan Nellie Wu, EECS (co-advised with Joel Emer)
Zi Yu Fisher Xue, EECS (co-advised with Joel Emer)

UNDERGRADUATE STUDENTS

Xavier Bell, AeroAstro
Kaustubh Dighe, EECS
Andrew Feldman, EECS
Sebastian Garcia, EECS
Michael Gilbert, EECS
Kailas Kahler, EECS
John Posada, AeroAstro
Sean Alex Rice, EECS
Adrianna Wojtyna, EECS
Reng Zheng, EECS

SUPPORT STAFF

Janice L. Balzer, Administrative Assistant

SELECTED PUBLICATIONS

T. Andrulis, J. Emer, and V. Sze, "RAELLA: Reforming the Arithmetic for Efficient, Low-Resolution, and Low-Loss Analog PIM: No Retraining Required!," *International Symposium on Computer Architecture (ISCA)*, Jun. 2023.

M. Gilbert, Y. N. Wu, A. Parashar, V. Sze, and J. Emer, "LoopTree: Enabling Exploration of Fused-layer Dataflow Accelerators," *IEEE International Symposium on Performance Analysis of Systems and Software (ISPASS)*, Apr. 2023

H.-Y. Lai, C. Sodini, V. Sze, and T. Heldt, "Individualized Tracking of Neurocognitive-State-Dependent Eye-Movement Features Using Mobile Devices," *Proceedings of the ACM on Interactive, Mobile, Wearable and Ubiquitous Technologies (IMWUT)*, Vol. 7, No. 1, pp. 1 – 23, Mar. 2023.

S. Sudhakar, V. Sze, S. and Karaman, "Data Centers on Wheels: Emissions from Computing Onboard Autonomous Vehicles," *IEEE Micro, Special Issue on Environmentally Sustainable Computing*, Vol. 43, No. 1, pp. 29 – 39, Jan./Feb. 2023.

Y. N. Wu, P. Tsai, A. Parashar, V. Sze, and J. Emer, "Sparseloop: An Analytical Approach to Sparse Tensor Accelerator Modeling," *ACM/IEEE International Symposium on Microarchitecture (MICRO)*, Oct. 2022.

Glossary

TECHNICAL ACRONYMS

ADC	Analog-to-Digital Converters
CMOS	Complementary Metal–Oxide–Semiconductor
CNT	Carbon Nanotubes
ECP	Electro-Chemical Plating
FET	Field-Effect Transistor
HSQ	Hydrogen Silsesquioxane
InFO	Integrated Fan Out
MOSFET	Metal–Oxide–Semiconductor Field-Effect Transistor
nTRON	Nanocryotron
RDL	Re-distribution Layers
RIE	Reactive Ion Etching
SNSPDs	Superconducting Nanowire Single Photon Detectors
SS	Subthreshold Swing
TMAH	Tetramethylammonium Hydroxide
TREC	Thermally Regenerative Electrochemical Cycle

MIT ACRONYMS & SHORTHAND

BE	Department of Biological Engineering
Biology	Department of Biology
ChemE	Department of Chemical Engineering
CICS	Center for Integrated Circuits and Systems
CMSE	Center for Materials Science and Engineering
↳IRG	Interdisciplinary Research Group
DMSE	Department of Materials Science & Engineering
EECS	Department of Electrical Engineering & Computer Science
ISN	Institute for Soldier Nanotechnologies
KI	David H. Koch Institute for Integrative Cancer Research
LL	Lincoln Laboratory
MAS	Program in Media Arts & Sciences
MechE	Department of Mechanical Engineering
MEDRC	Medical Electronic Device Realization Center
MIT-CG	MIT/MTL Center for Graphene Devices and 2D Systems
MITEI	MIT Energy Initiative
MIT-GaN	MIT/MTL Gallium Nitride (GaN) Energy Initiative

MISTI	MIT International Science and Technology Initiatives
MIT-SUTD	MIT-Singapore University of Technology and Design Collaboration Office
MIT Skoltech	MIT Skoltech Initiative
MTL	Microsystems Technology Laboratories
NSE	Department of Nuclear Science & Engineering
Physics	Department of Physics
Sloan	Sloan School of Management
SMA	Singapore-MIT Alliance
↳**SMART**	Singapore-MIT Alliance for Research and Technology Center
↳**SMART-LEES**	SMART Low Energy Electronic Systems Center
SUTD-MIT	MIT-Singapore University of Technology and Design Collaboration Office
UROP	Undergraduate Research Opportunities Program

U.S. GOVERNMENT ACRONYMS

AFOSR	U.S. Air Force Office of Scientific Research
↳**FATE-MURI**	Foldable and Adaptive Two-dimensional Electronics Multidisciplinary Research Program of the University Research Initiative
AFRL	U.S. Air Force Research Laboratory
ARL	U.S. Army Research Laboratory
↳**ARL-CDQI**	U.S. Army Research Laboratory Center for Distributed Quantum Information
ARO	Army Research Office
ARPA-E	Advanced Research Projects Agency - Energy (DOE)
DARPA	Defense Advanced Research Projects Agency
↳**DREaM**	Dynamic Range-enhanced Electronics and. Materials
DoD	Department of Defense
DoE	Department of Energy
↳**EFRC**	U.S. Department of Energy: Energy Frontier Research Center (Center for Excitonics)
DTRA	U.S. DoD Defense Threat Reduction Agency
IARPA	Intelligence Advanced Research Projects Activity
↳**RAVEN**	Rapid Analysis of Various Emerging Nanoelectronics
NASA	National Aeronautics and Space Administration
↳**GSRP**	NASA Graduate Student Researchers Project
NDSEG	National Defense Science and Engineering Graduate Fellowship
NIH	National Institutes of Health
↳**NCI**	National Cancer Institute
NNSA	National Nuclear Security Administration

NRO	National Reconnaissance Office
NSF	National Science Foundation
↳**CBMM**	NSF Center for Brains, Minds, and Machines
↳**CIQM**	Center for Integrated Quantum Materials
↳**CSNE**	NSF Center for Sensorimotor Neural Engineering
↳**E3S**	NSF Center for Energy Efficient Electronics Science
↳**GRFP**	Graduate Research Fellowship Program
↳**IGERT**	NSF The Integrative Graduate Education and Research Traineeship
↳**NEEDS**	NSF Nano-engineered Electronic Device Simulation Node
↳**PECASE**	Presidential Early Career Awards for Scientists and Engineers
↳**SEES**	NSF Science, Engineering, and Education for Sustainability
↳**STC**	NSF Science-Technology Center
ONR	Office of Naval Research

OTHER ACRONYMS

CNRS Paris	Centre National de la Recherche Scientifique
CONACyT	Consejo Nacional de Ciencia y Tecnología (Mexico)
IEEE	Institute of Electrical and Electronics Engineers
IHP Germany	Innovations for High Performance Microelectronics Germany
KIST	Korea Institute of Science and Technology
KFAS	Kuwait Foundation for the Advancement of Sciences
MASDAR	Masdar Institute of Science and Technology
NTU	Nanyang Technological University
NUS	National University of Singapore
NYSCF	The New York Stem Cell Foundation
SRC	Semiconductor Research Corporation
↳**NEEDS**	NSF/SRC Nano-Engineered Electronic Device Simulation Node
SUTD	Singapore University of Technology and Design
TEPCO	Tokyo Electric Power Company
TSMC	Taiwan Semiconductor Manufacturing Company

IN APPRECIATION OF OUR MICROSYSTEMS INDUSTRIAL GROUP MEMBER COMPANIES:

Analog Devices, Inc.
Applied Materials
Draper
Edwards
HARTING
Hitachi High-Tech Corporation
IBM Research
Lam Research
NEC
TSMC
Texas Instruments

AND MIT.NANO CONSORTIUM MEMBER COMPANIES:

Analog Devices, Inc.
Draper
Edwards
Fujikura
IBM Research
Lam Research
NCSOFT
NEC
Raith
UpNano

MTL MICROSYSTEMS TECHNOLOGY LABORATORIES

MIT.nano