Research Overview

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Research Topics

- Continutous-time pipeline ADC (2nd Generation)
- Secure A/D converters (in collaboration with A. Chandrakasan)
- Analog In-Memory Computing
- Tissue perfusion pressure modeling and measurements (in collaboration with C. Sodini, and Dr. A. Aguirre, MGH)
- Tissue perfusion in glaucoma patients (new, in collaboration with C. Sodini, and T. Heldt)
- Electronic bacterial sensing(in collaboration with M. Shulaker)

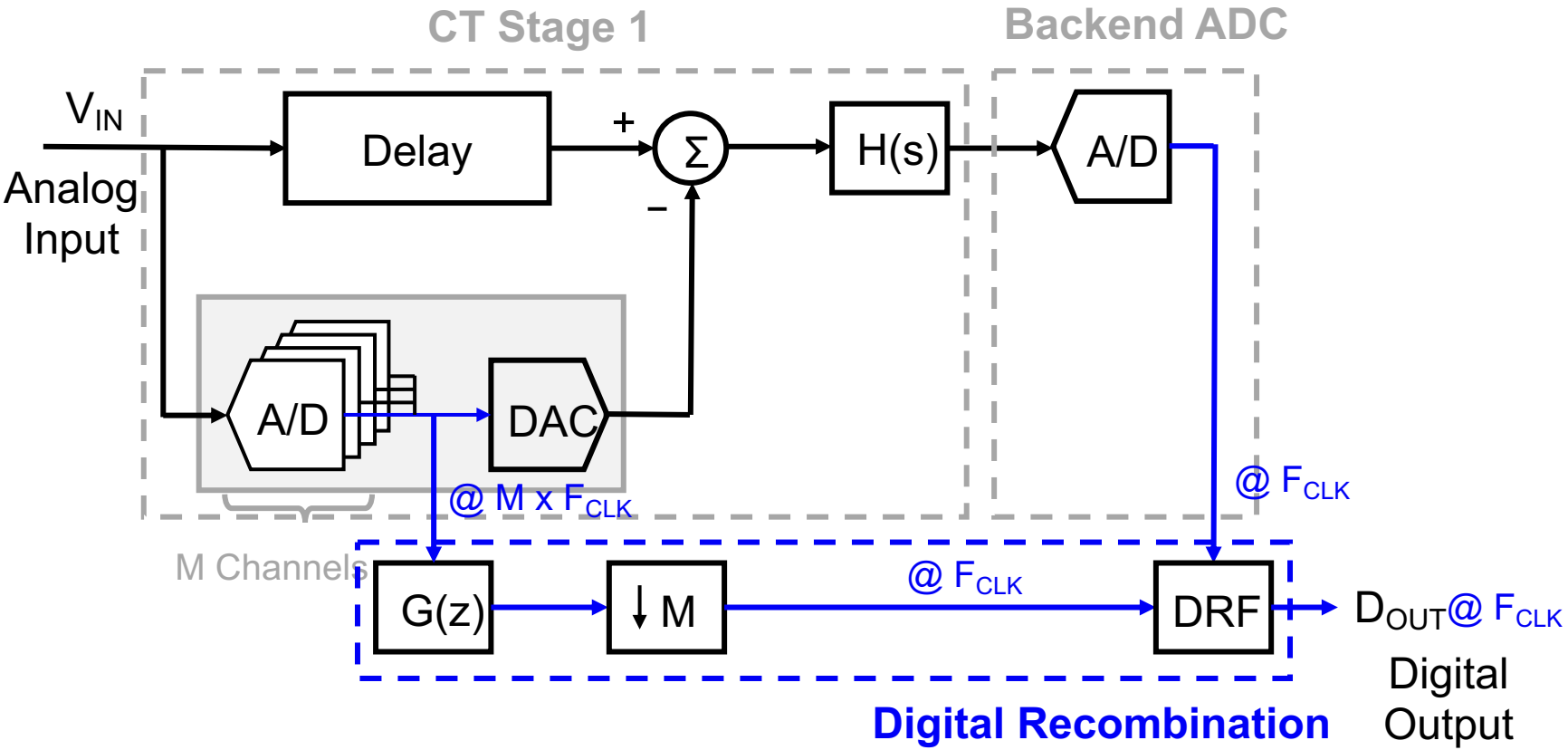
Continuous-Time Pipeline (CTP) ADC with Reduced Clock Jitter Sensitivity

Rishabh Mittal, Anantha Chandrakasan, and Hae-Seung Lee (MIT)

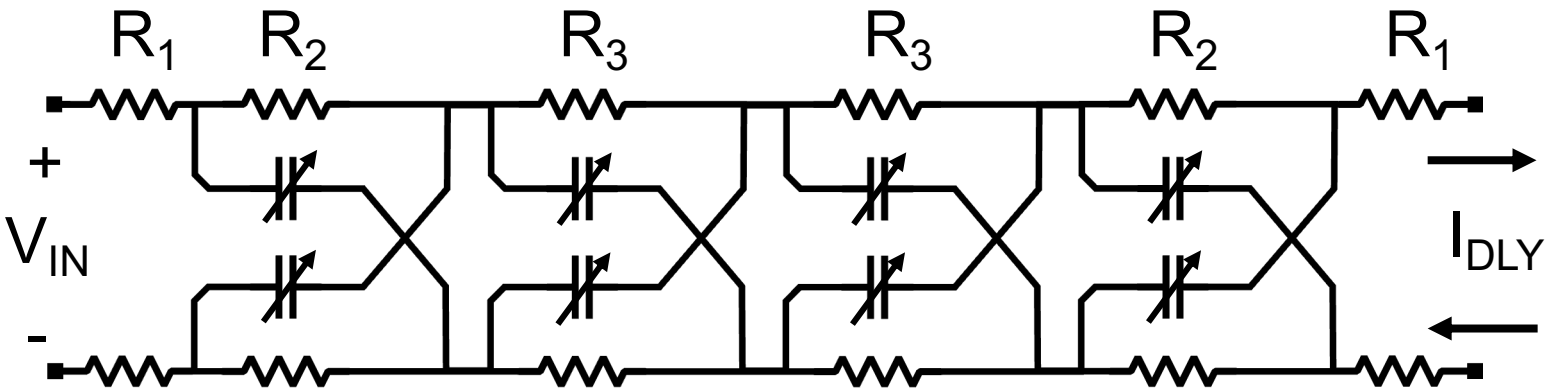
Hajime Shibata, Sharvil Patil (ADI)

Gabriele Manganaro (MediaTek)

Time-Interleaved sub-ADC-DAC Path

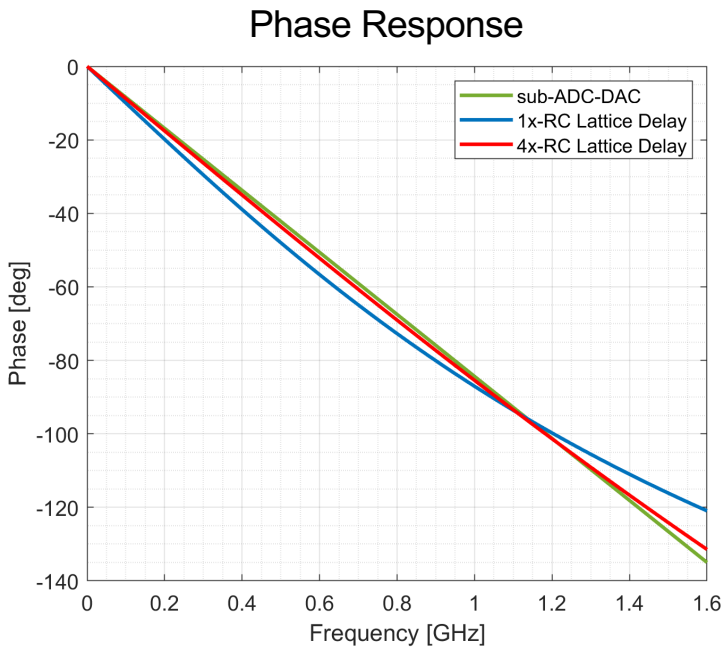


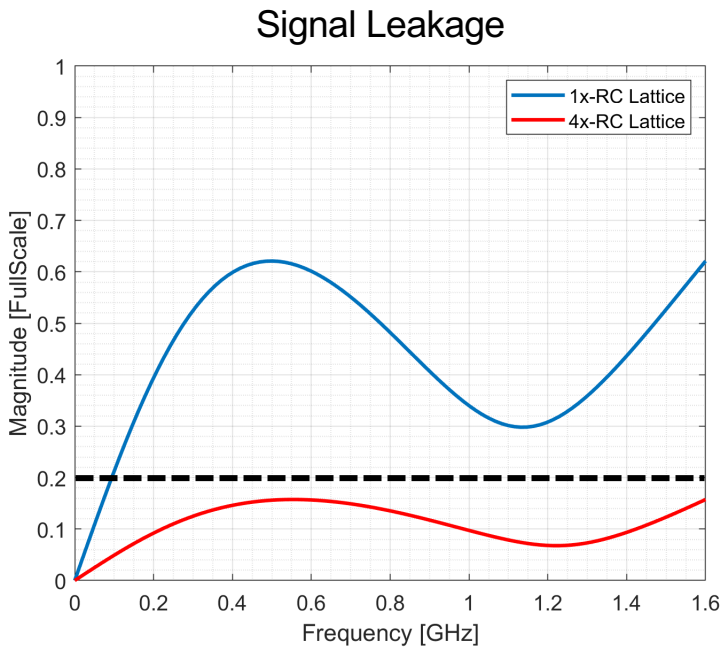
Proposed Delay Line



- 4x-cascaded RC-lattice-based delay line: no inductors
- Good phase matching, suitable up to 1.6 GHz BW

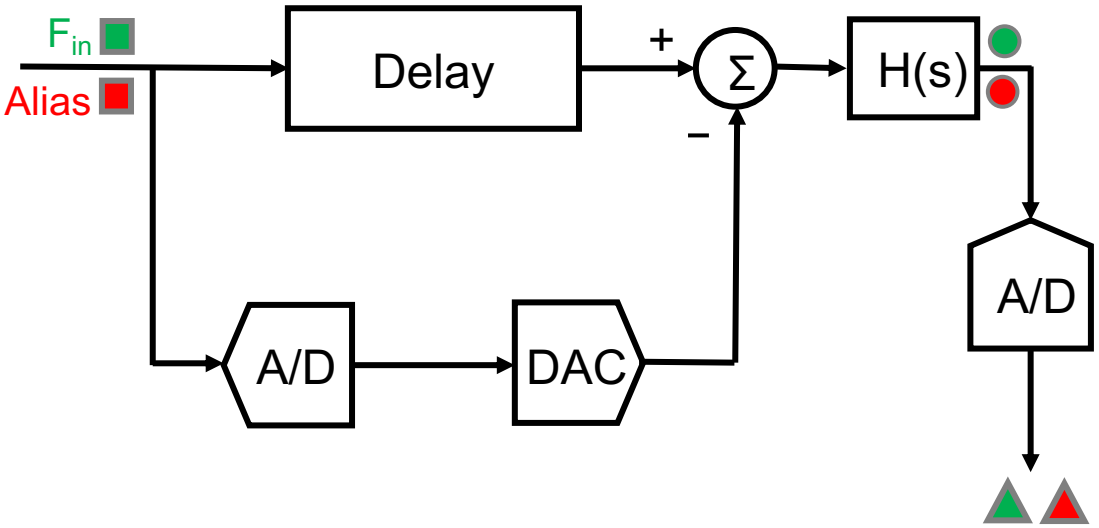
Phase Response and Signal Leakage

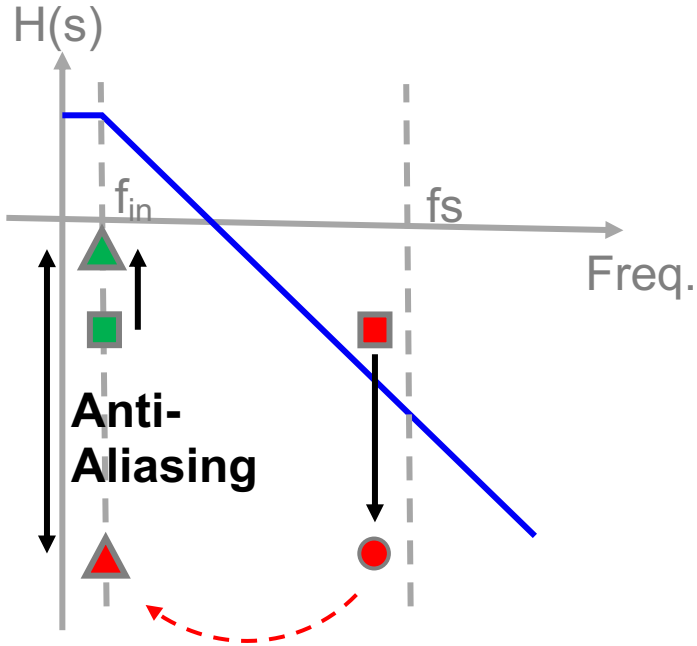




In the above plots we assume that both 1x- and 4x-RC lattice delay lines have been optimized for 1.6 GHz BW operation (i.e., all R and C values are chosen such that signal leakage is minimized in-band)

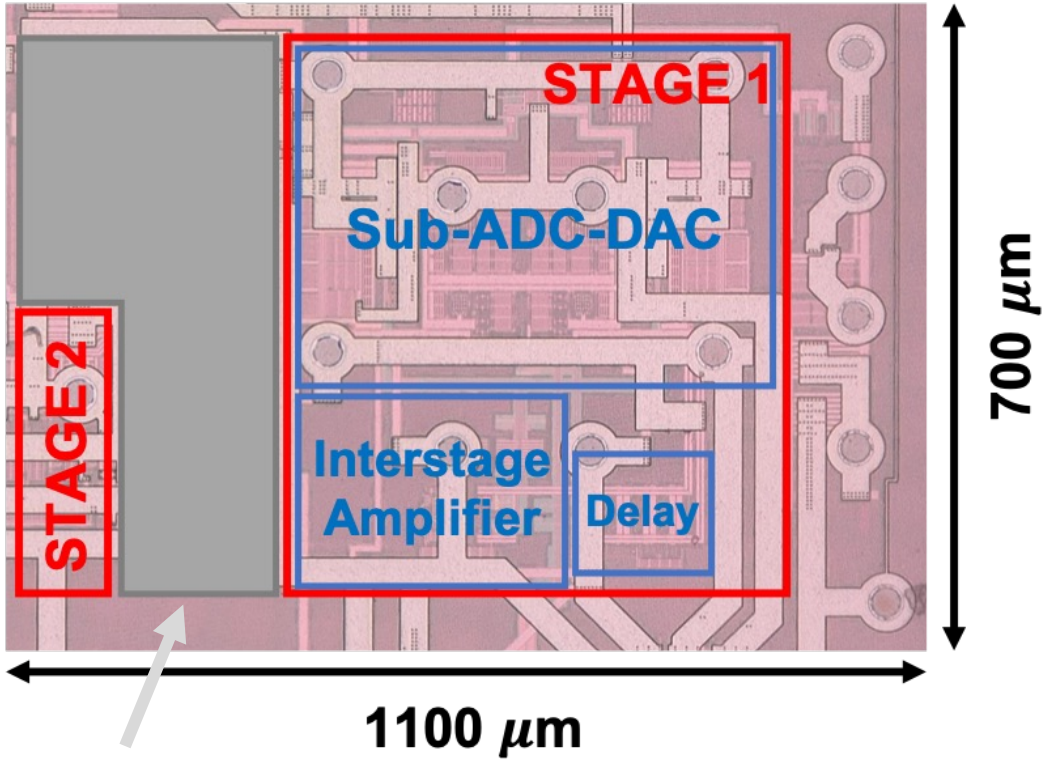
Anti-Aliasing in CT Pipeline ADC





$$\text{Anti-Aliasing} \approx \frac{H(f_S - f_{in})}{H(f_{in})}$$

Die Photo

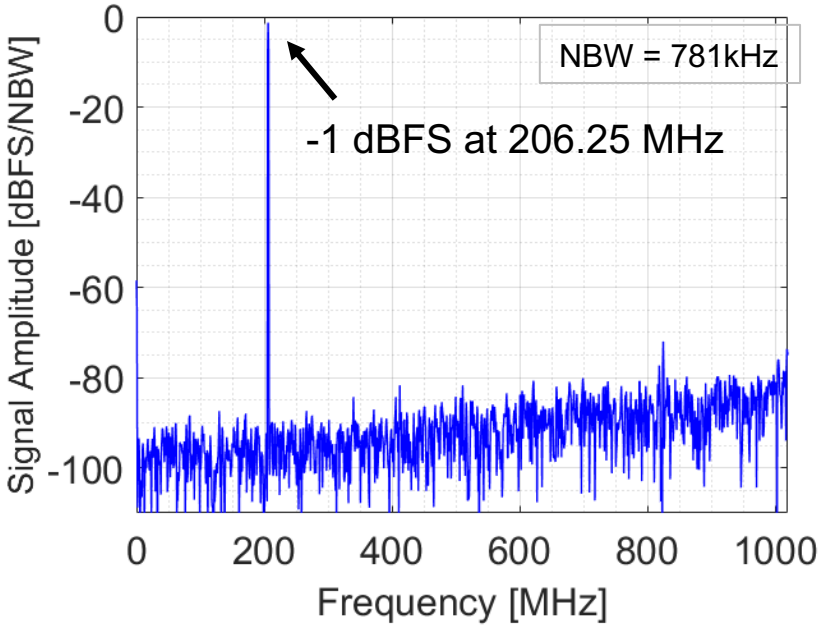


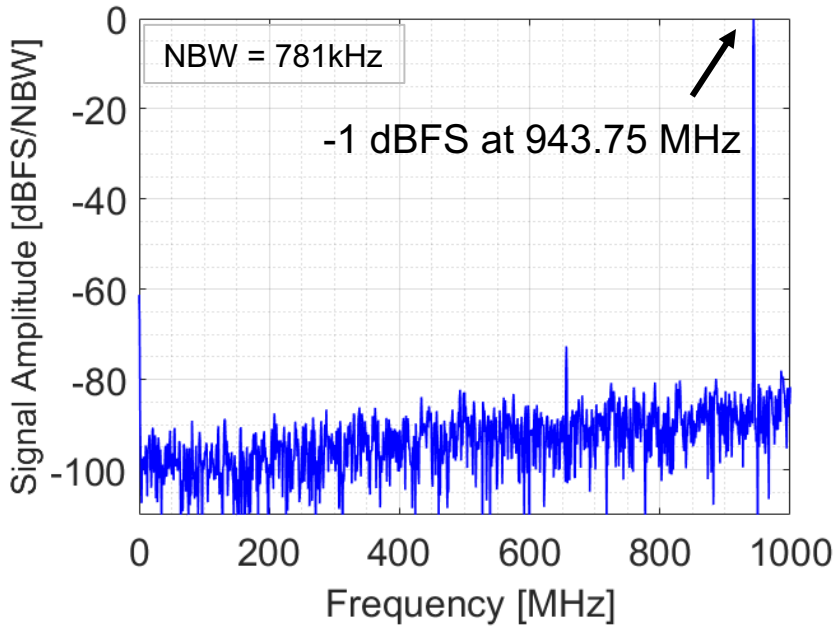
Part of a shared tapeout

- Technology : 16nm FinFET
- Area of ADC core: 0.77 mm^2
- Digital recombination is performed off-chip
  - Estimated area* = 0.15 – 0.17 mm^2
  - Estimated power* = 113 mW

* Digital recombination area and power estimates are based on [4].

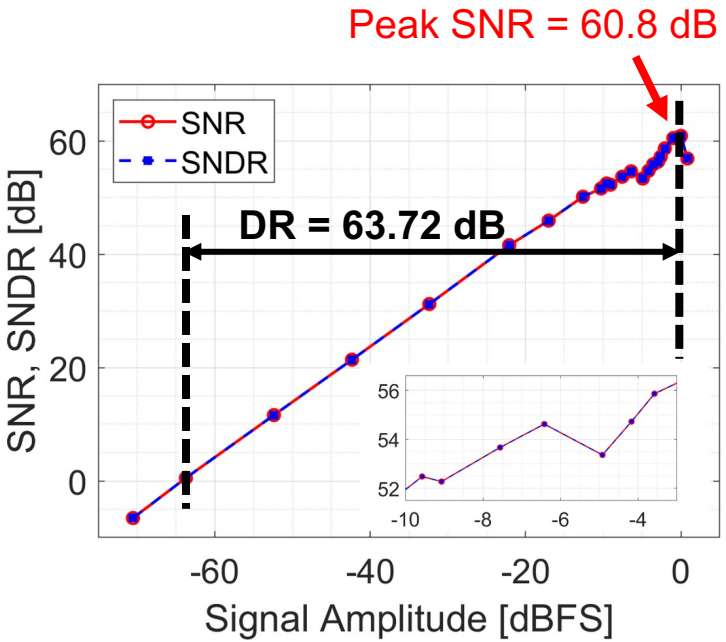
Measured Spectrum



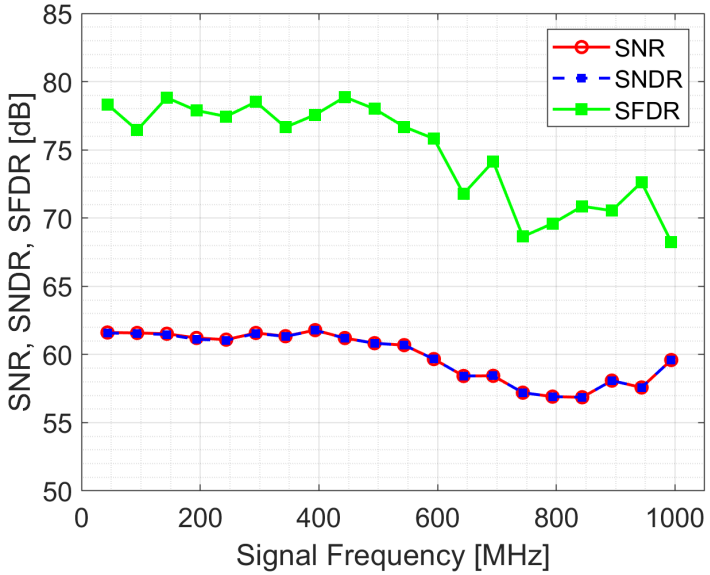


- F_{CLK} = 6.4 GHz
- Small-signal average NSD = -151.7 dBFS/Hz.
- Noise floor is 1st-order shaped due to backend VCO-ADC noise [4].

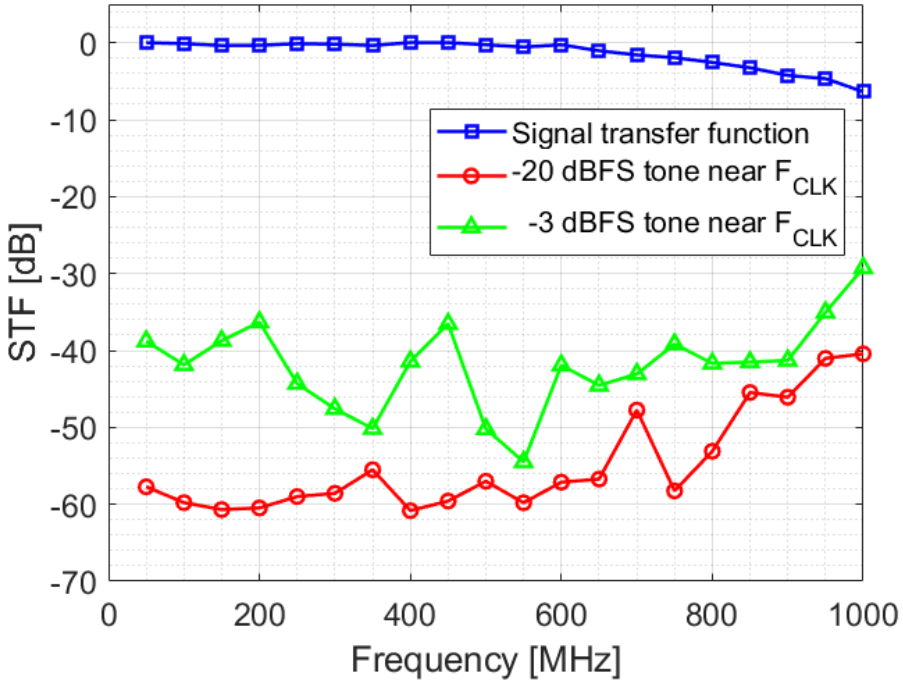
Measured SNR, SNDR and SFDR



F_{IN} = 993.75 MHz



Measured STF and Anti-Aliasing



Small amplitude interferer
Anti-aliasing > 40 dB

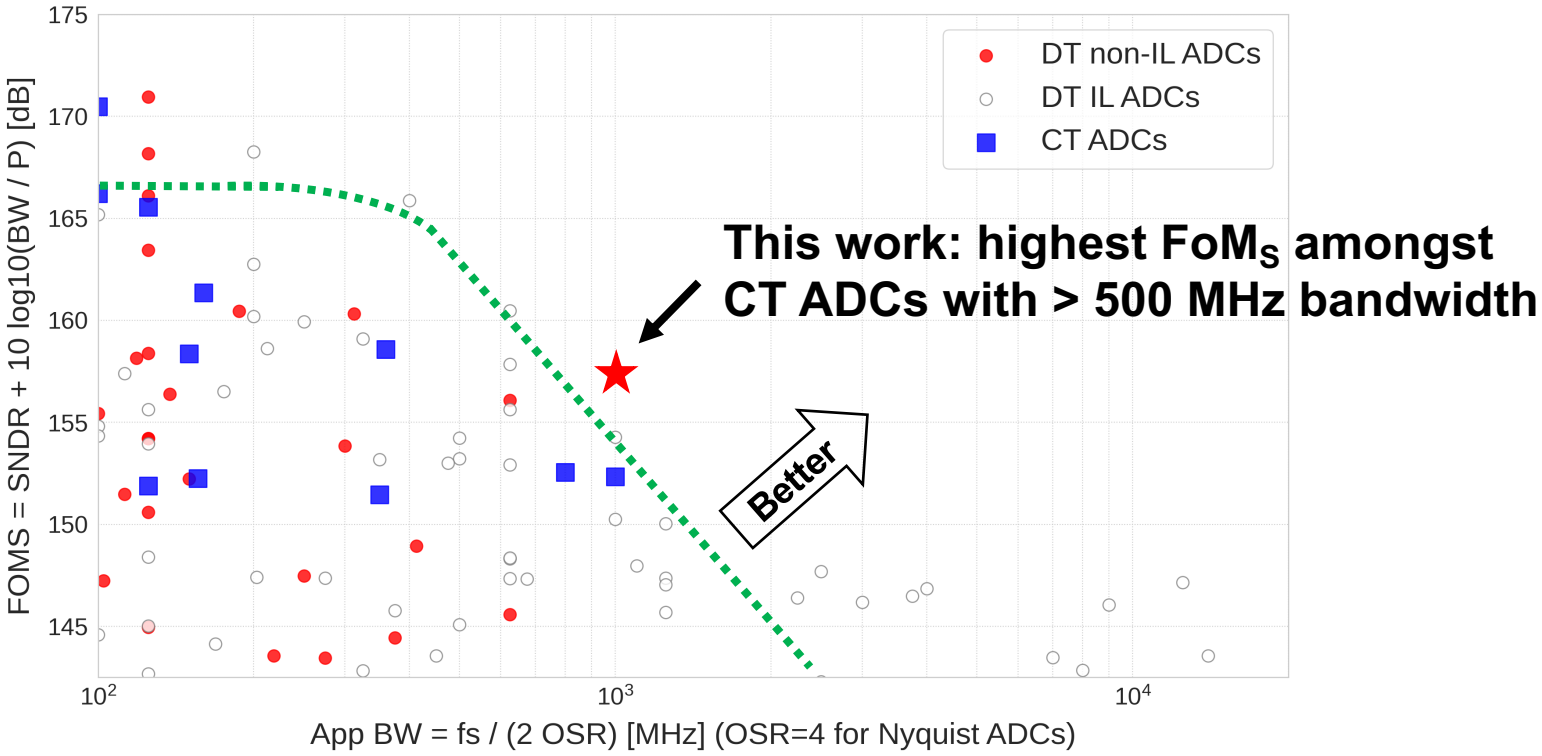
Large amplitude interferer
Anti-aliasing > 29 dB

[interferer near F_{CLK} = 6.4 GHz]

Performance Comparison

	This work	ISSCC 2020	JSSC 2017	TCAS-I 2022	JSSC 2010	ISSCC 2017	JSSC 2016
Architecture	**CT Pipeline Interleaved**	CT Pipeline VCO-based	CT Pipeline Multistage	CT Pipeline w/ Decimation	CT Pipeline	DT Pipeline Interleaved	CT MASH ΔΣ
Technology	**16 nm FinFET**	16 nm FinFET	28 nm CMOS	65 nm CMOS	180 nm CMOS	28 nm CMOS	28 nm CMOS
f_S [MHz]	**6400**	6400	9000	800	26	10000	8000
OSR	**3.2**	4	4	4	2	1.5	8.6
BW [MHz]	**1000**	800	1125	100	6.5	3300	465
Peak SNR/SNDR [dB]	**61.7**	58	65.4	70.4 / 70	62.7 / 61.1	56 / 55	68
SFDR [dB]	**68**	73	73	-	67	71	83
HD2 [dB]	**< -84.7**	-93	-79	-79.7	-66	-77	-90
HD3 [dB]	**< -80.3**	-84	-86	< -77.2	-	-73	-86
DR [dB]	**63.7**	60	73	73	-	60	72
Inherent Anti-Aliasing	**Yes**	Yes	Yes	Yes	Yes	No	Yes
Power [mW]	**240**	280	2330	29	26.7	2900	350
Area [mm^2]	**0.77**	0.34	5.1	0.77	1.9	7.4	1.2
FoM_S = SNDR + $10\log_{10}(BW/P)$ [dB]	**157.9**	152.5	152.2	165.4	145	147	155

Schrier Figure-of-Merit Comparison



Advantages of Continuous-Time ADCs

- Inherent anti-aliasing due to lack of lead sample-and-hold
  - Anti-alias filter may be unnecessary
  - Delay line amplitude and phase matching is critical for anti-aliasing large amplitude blockers
- The effect of clock jitter can be reduced by time-interleaving 1st stage sub-ADC/DAC
- Time-interleaving also improves the ADC bandwidth and anti-aliasing

2nd Gen Research topics

- Extend CTP to higher bandwidth
- High-frequency analog delay line for amplitude and phase matching and small area
  - Multiple-path RC cascades
  - On-chip transmission line
  - Wavelength reduction technique
- Further mitigation of DAC clock jitter by “shaping” DAC pulses
- Increase time-interleaving factor
- Incorporation of filtering function in the ADC