Research Overview

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Research Topics, I

- Ultra-low power SAR with energy efficient search (in collaboration with A. Chandrakasan, Completed)
- Ultrasound measurement for absolute ABP and Hemodynamics using machine learning (in collaboration with C. Sodini,S. Han, and A. Aguirre)
- Direct Hybrid Encoding SAR ADC for Analog Neural Networks (in collaboration with A. Chandrakasan, HT Kung, Harvard)
- Dual threshold ADC for activity scaling and security (in collaboration with A. Chandrakasan)
- Nanochannel protein sensing (in collaboration with R. Ram)
- 3rd generation molecular clock (in collaboration with R. Han)

Research Topics, II

- Jitter tolerant pipeline ADC (in collaboration with A. Chandrakasan, Gabriele Manganaro, Hajime Shibata, ADI)
- Bandgap-free temperature sensor (in collaboration with A. Chandrakasan)
- Secure A/D converters (in collaboration with A. Chandrakasan, Completed)
- CNT pipeline ADCs (in collaboration with M. Shulaker)

Recode then LSB-first ADC

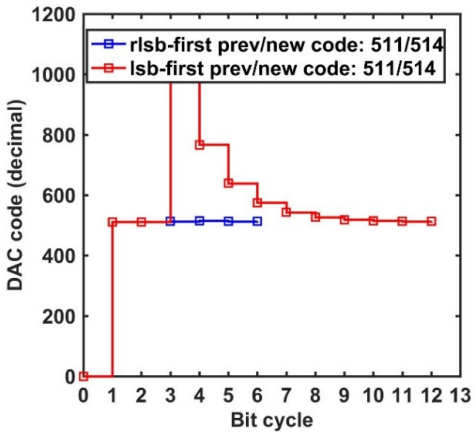
H. Singh, A. Chandrakasan and H.-S. Lee

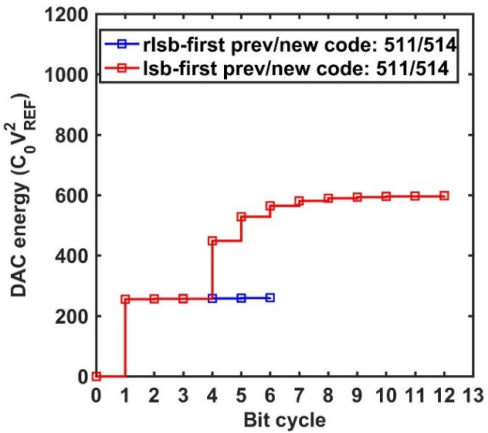
Split-DAC (SDAC) architecture

Energy efficient DAC switching by using Split DAC redundancy for initial voltage level of Vref/2

Recode then LSB-first (RLSB-first)

- Algorithm
  - **Recode** previous code to a code more favorable for LSB-first using SDAC code redundancy
  - **Sample** input
  - **Initialize** DAC to the encoded previous code
  - Do **LSB-first**
  - **Decode** current code
- **All small code transitions are efficient**

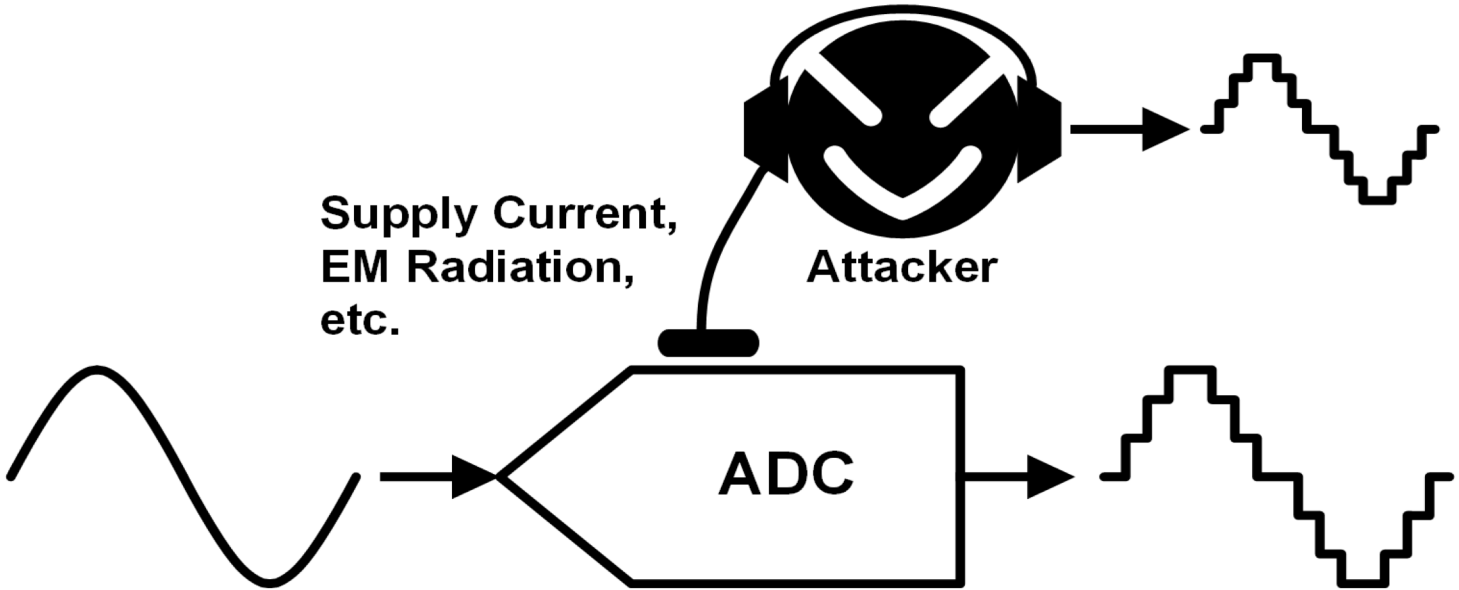




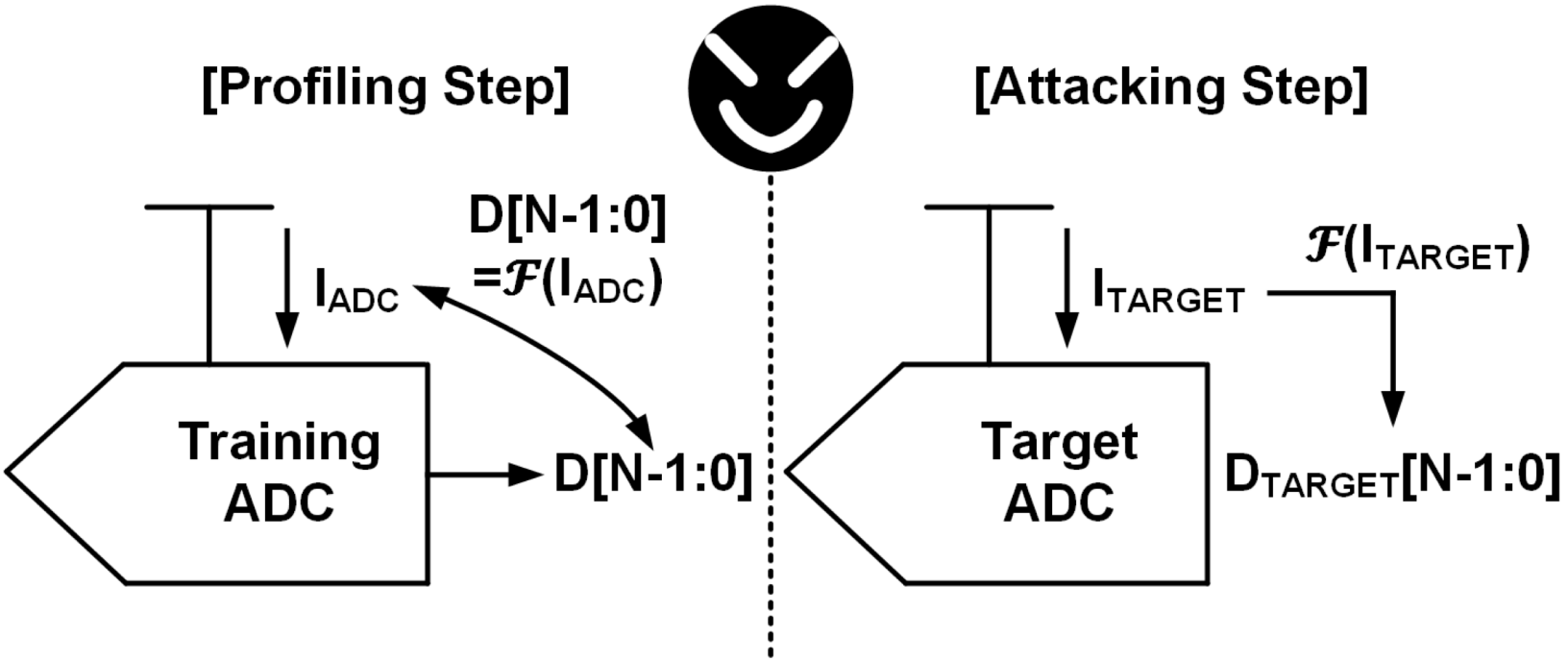
Secure ADCs

T. Jeong, A. Chandrakasan and H.-S. Lee

ADCs May Create a Security Loophole

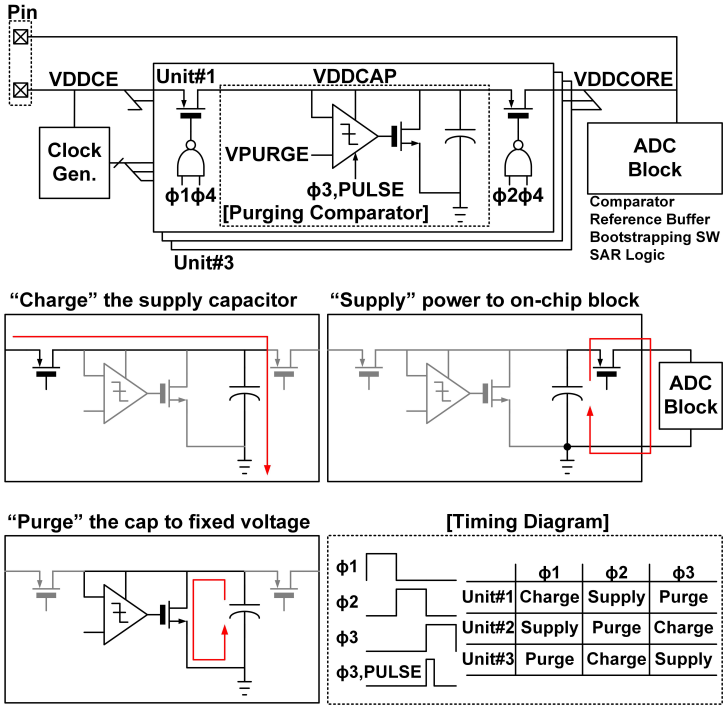


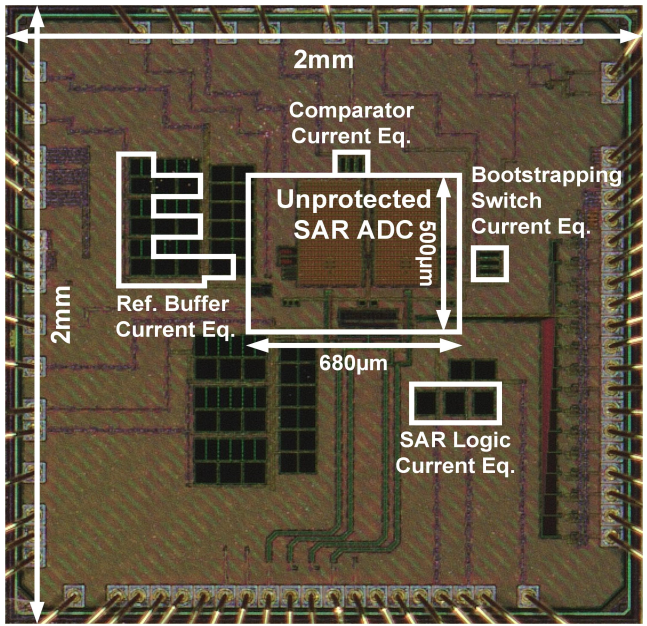
ADC PSA Method



- #1: Profiling step – Use training ADC to obtain D[N-1:0] =$\mathcal{F}$(I$_{ADC}$)
- #2: Attacking step – $\mathcal{F}$(*) to decode I$_{TARGET}$

ADC PSA Protection



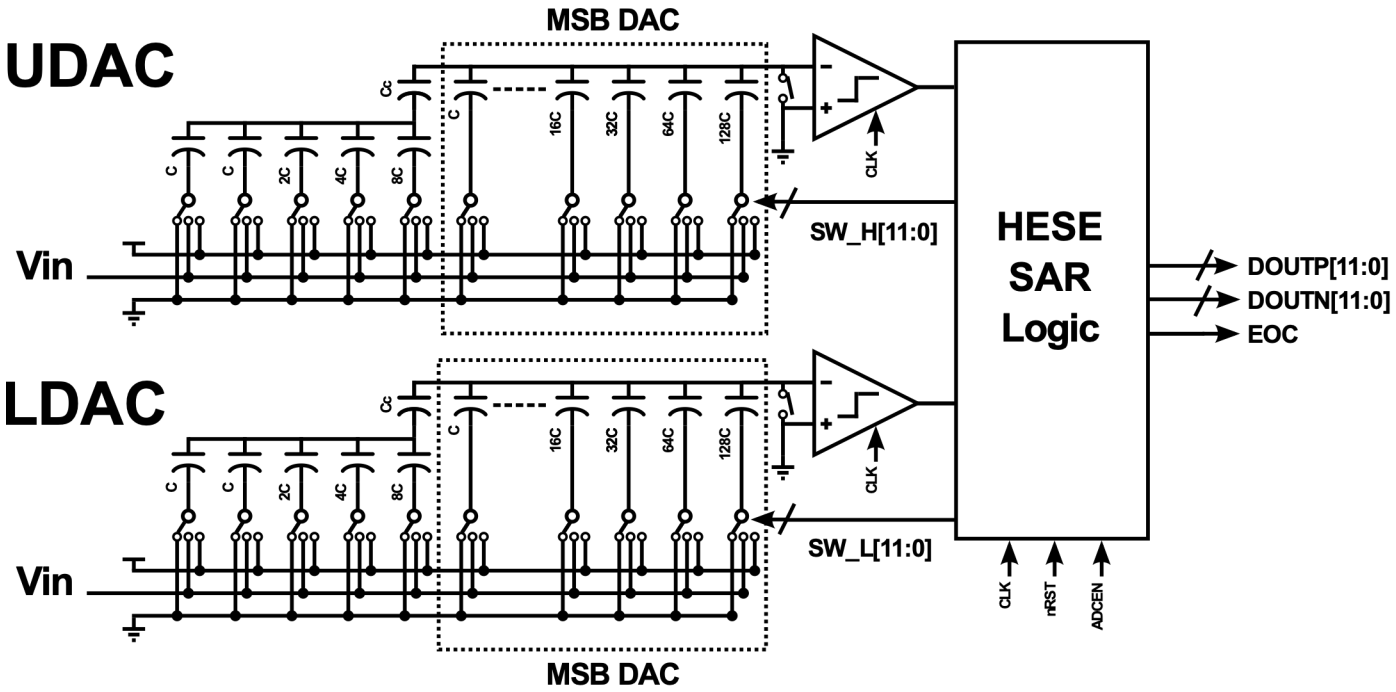


- Current equalizers to hide activities from power supply traces
- Protects both Vdd and GND traces from PSA

(C. Tokunaga and D. Blaauw, "Secure AES Engine with A Local Switched-Capacitor Current Equalizer," in ISSCC 2009, pp. 64–65.)

Direct HESE/Activity Scaling/Secure ADC (New)

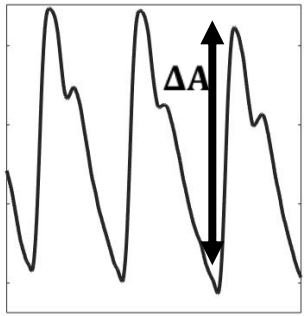
R. Chen, A. Chandrakasan and H.-S. Lee

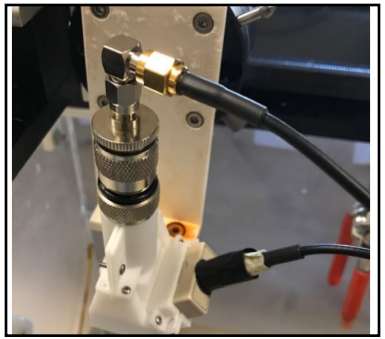


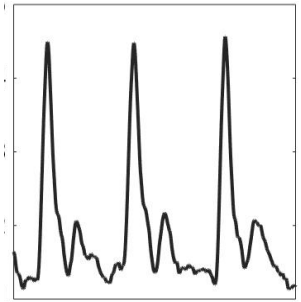
Single-ended 12 bits model; Bottom Plate Sampling; 8-4 Segmented DAC

Absolute Arterial Blood Pressure Estimation

Anand Chandrasekhar, Aaron Aguirre, Charles Sodini, Hae –Seung Lee
Hanrui Wang, Song Han



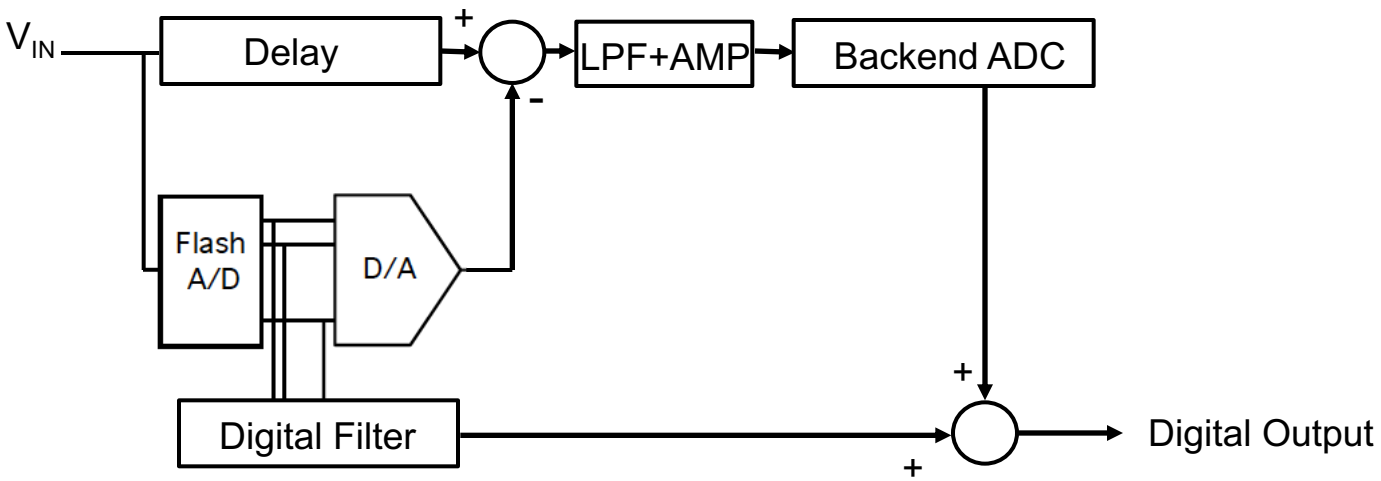




- **From A and V, the arterial compliance (or PWV) can be measured**
- **Using compliance, pulse pressure can be obtained from area waveform**
- **Absolute pressure requires calibration (e.g. cuff measurement)**
- **Transmission line model can be used to estimate absolute mean arterial pressure**
- **Machine learning method improves accuracy**

Clock Jitter Tolerant Pipeline ADC

Rishabh Mittal, A. Chandrakasan, H.–S. Lee
G. Manganaro (MediaTek), H. Shibata (ADI)

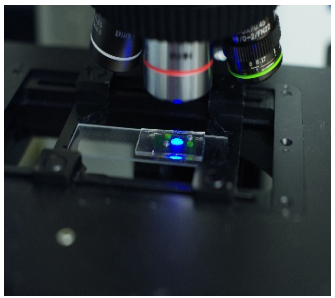


- Increased tolerance to clock jitter compared with conventional DT or CT pipeline
- Reduced residue
- Inherent antialiasing even with Nyquist backend

CMOS Nanofluidics for Protein Sensing

Collaboration with Prof. Rajeev J. Ram

Current lab-on-chip devices require bulky readout optics or electronics, which limit miniaturization.

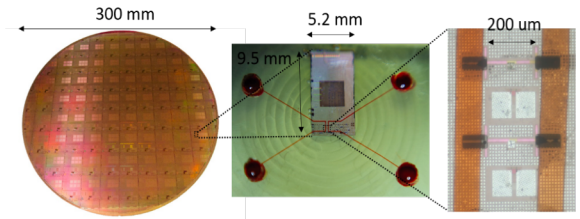


Goal: low-cost miniaturized protein sensors for:

1. Exacerbation prediction/prevention in chronic disease patients
2. Monitoring of therapeutic cells for pharmaceutical manufacturing
3. Closed-loop controlled agriculture

CMOS Nanofluidics for Protein Sensing, II

Integration of nanofluidics in CMOS enables the low cost manufacturing of monolithic protein sensors.



100 nm high nanochannels are integrated alongside readout detectors and circuits

Circuit challenge: readout circuit must sense tiny resistance change in large nanochannel resistance (high noise)